

Automated Discovery of Invertibility Conditions via Syntax-Guided Synthesis

Andrew Reynolds

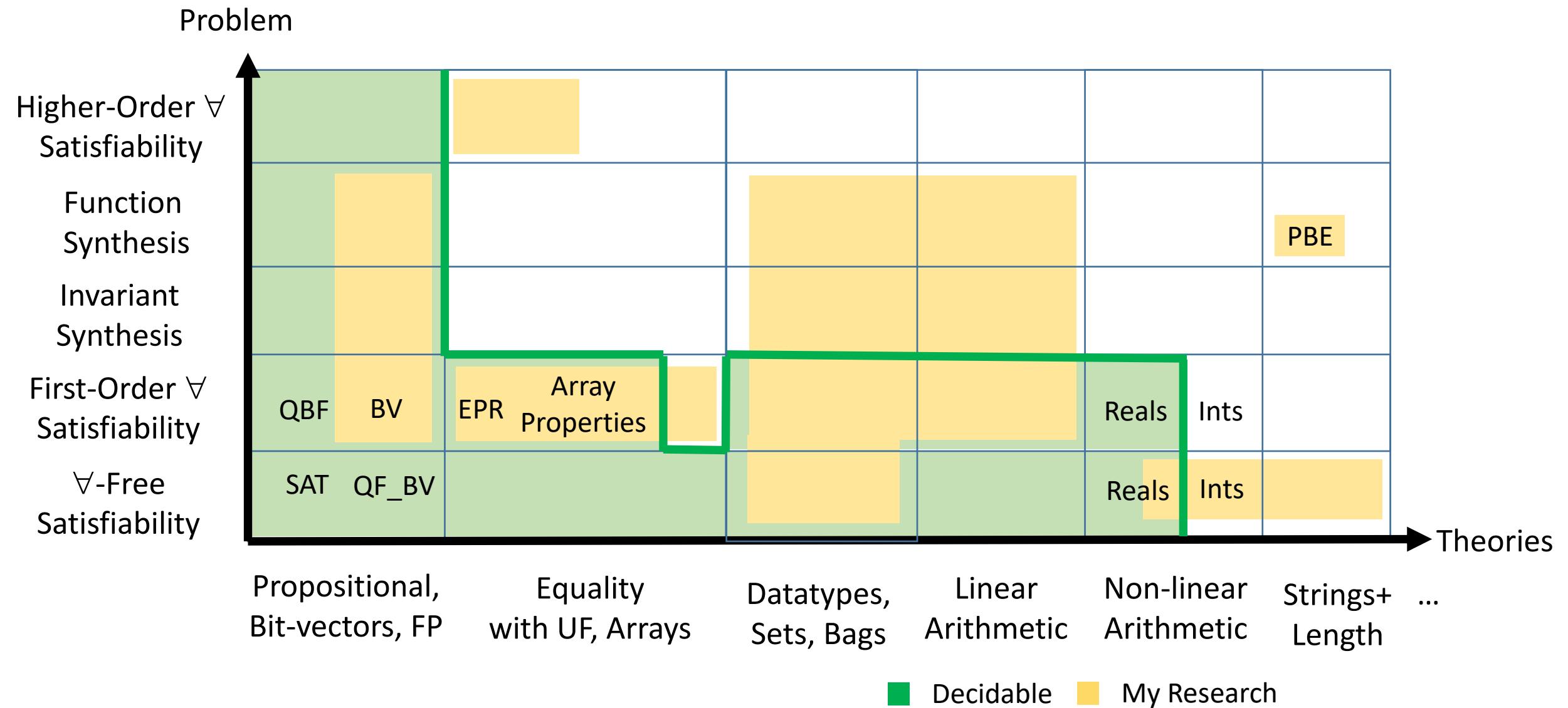
Dec 2, 2021



My Research

- Satisfiability Modulo Theories (SMT) Solvers
 - Fully automated reasoners with many applications
 - Verification, Synthesis, Symbolic Execution, Theorem Proving, Security Analysis
- Development of the SMT solver cvc5
 - Open source, available at : <https://cvc5.github.io/>
- Acknowledgements:
 - Cesare Tinelli, Clark Barrett, Haniel Barbosa, Andres Noetzli, Aina Niemetz, Mathias Preiner
 - Rest of cvc5 development team (past and present)
 - Viktor Kuncak

SMT Solvers: Standalone Tools for Many Problems



In this Talk:

- Using *Syntax-Guided Synthesis* (SyGuS) to aid SMT solver development
- How we use SyGuS for developing cvc5:
 - Discovering rewrite rules [[Noetzli et al SAT 2019](#)]
 - Automatic test case generation
 - Discovering Invertibility Conditions for Bit-Vectors [[Niemetz et al CAV 2018](#)]
 - Discovering Invertibility Conditions for *Floating Points* [[Brain et al CAV 2019](#)]

How does Syntax-Guided Synthesis work?

Synthesis Conjectures

$$\exists f. \forall x. P(f, x)$$



There exists a function f for which **property** P holds for all x

Syntax-Guided Synthesis Conjectures Modulo T

$$\exists f. \forall x. P(f, x)$$


$\text{spec}(f)$

There exists a function f for which **property** P holds for all x

$$A \rightarrow A + A \mid -A \mid x \mid y \mid 0 \mid 1 \mid \text{ite}(B, A, A)$$
$$B \rightarrow B \wedge B \mid \neg B \mid A = A \mid A \geq A \mid \perp$$


$\text{syntax}(f)$

The body of f is generated by the above **grammar** with start symbol A

\Rightarrow *Syntax-guided synthesis “SyGuS” [Alur et al 2013]*

Enumerative Cex-Guided Inductive Synthesis (CEGIS)

```
syntax(f) :  
A->A+A|-A|x|y|0|1|ite(B,A,A)  
B->B&B|¬B|A=A|A≥A|⊥
```

```
spec(f) :  
∀xy.f(x,y)=f(y,x)+f(0,1)
```

Solution
Enumerator

Solution
Verifier

Enumerative Cex-Guided Inductive Synthesis (CEGIS)

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spec(f) :  
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```

Solution
Enumerator

Solution
Verifier

$f := \lambda xy . x ?$

Enumerative Cex-Guided Inductive Synthesis (CEGIS)

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syntax(f) :  
A->A+A|-A|x|y|0|1|ite(B,A,A)  
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```

```
spec(f) :  
∀xy. f(x,y)=f(y,x)+f(0,1)
```

Solution
Enumerator

Solution
Verifier

$$f(0,1) = f(1,0) + f(0,1)$$

$$f := \lambda xy . x?$$

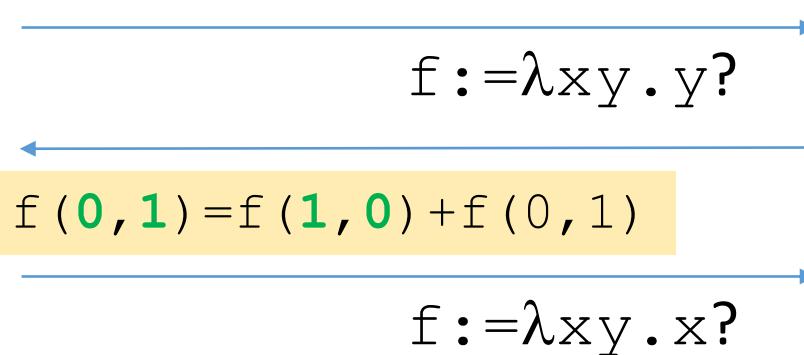
..counterexample: spec does not hold for $(x,y)=(0,1)$

Enumerative Cex-Guided Inductive Synthesis (CEGIS)

syntax (f) :
 $A \rightarrow A + A \mid -A \mid x \mid y \mid 0 \mid 1 \mid \text{ite}(B, A, A)$
 $B \rightarrow B \wedge B \mid \neg B \mid A = A \mid A \geq A \mid \perp$

spec (f) :
 $\forall xy. f(x, y) = f(y, x) + f(0, 1)$

Solution
Enumerator



...new candidate $\lambda xy. y$ satisfies $(x, y) = (0, 1)$

Enumerative Cex-Guided Inductive Synthesis (CEGIS)

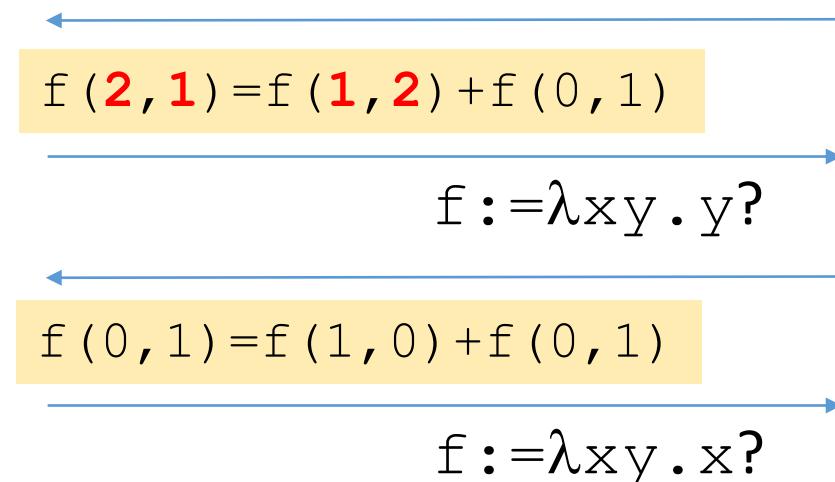
syntax (f) :

$$A \rightarrow A + A \mid -A \mid x \mid y \mid 0 \mid 1 \mid \text{ite}(B, A, A)$$
$$B \rightarrow B \wedge B \mid \neg B \mid A = A \mid A \geq A \mid \perp$$

spec (f) :

$$\forall xy. f(x, y) = f(y, x) + f(0, 1)$$

Solution
Enumerator



...counterexample: spec does not hold for $(x, y) = (2, 1)$

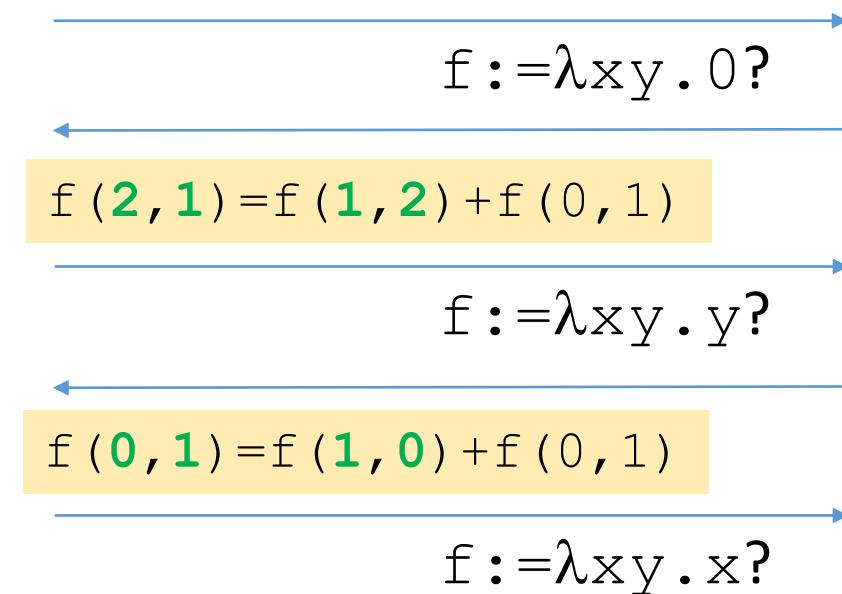
Enumerative Cex-Guided Inductive Synthesis (CEGIS)

syntax (f) :
 $A \rightarrow A + A \mid -A \mid x \mid y \mid 0 \mid 1 \mid \text{ite}(B, A, A)$
 $B \rightarrow B \wedge B \mid \neg B \mid A = A \mid A \geq A \mid \perp$

spec (f) :
 $\forall xy. f(x, y) = f(y, x) + f(0, 1)$

Solution
Enumerator

Solution
Verifier



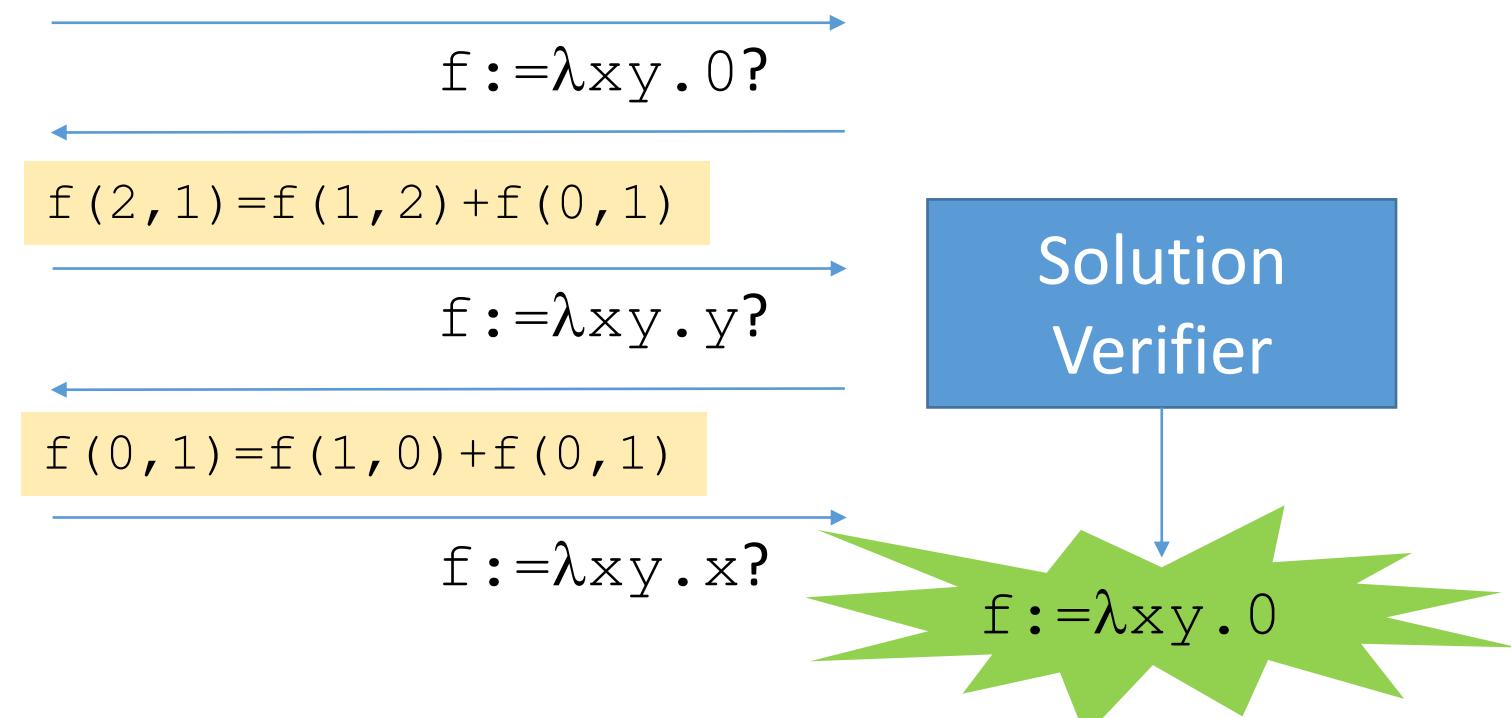
...new candidate $\lambda xy. 0$ satisfies $(x, y) = (0, 1), (2, 1)$

Enumerative Cex-Guided Inductive Synthesis (CEGIS)

syntax (f) :
 $A \rightarrow A + A \mid -A \mid x \mid y \mid 0 \mid 1 \mid \text{ite}(B, A, A)$
 $B \rightarrow B \wedge B \mid \neg B \mid A = A \mid A \geq A \mid \perp$

spec (f) :
 $\forall xy. f(x, y) = f(y, x) + f(0, 1)$

Solution
Enumerator



...new candidate $\lambda xy. 0$ has no counterexamples wrt **spec (f)**

Enumerative Cex-Guided Inductive Synthesis (CEGIS)

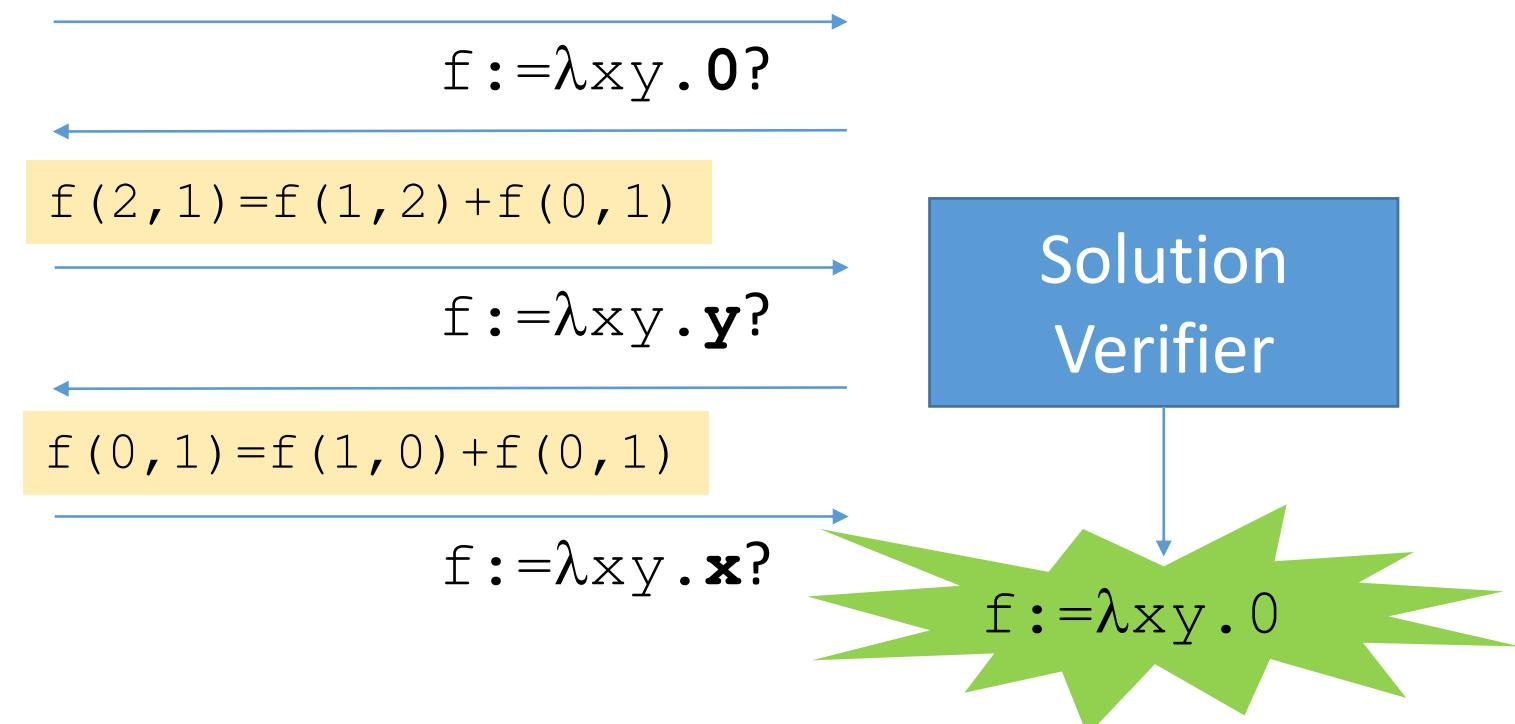
syntax (f) :

$A \rightarrow A + A \mid -A \mid x \mid y \mid 0 \mid 1 \mid \text{ite}(B, A, A)$
 $B \rightarrow B \wedge B \mid \neg B \mid A = A \mid A \geq A \mid \perp$

spec (f) :

$\forall xy. f(x, y) = f(y, x) + f(0, 1)$

Solution
Enumerator



⇒ Terms $x, y, 0, \dots$ are a (fair) **enumeration** of terms generated by **syntax (f)**

CEGIS using SMT solvers

```
syntax(f) :  
A->A+A|-A|x|y|0|1|ite(B,A,A)  
B->B&B|¬B|A=A|A≥A|⊥
```

```
spec(f) :  
∀xy.f(x,y)=f(y,x)+f(0,1)
```

Solution
Enumerator

SMT Solver
Solution
Verifier

CEGIS inside an SMT solver

```
syntax(f) :  
A->A+A|-A|x|y|0|1|ite(B,A,A)  
B->B&B|¬B|A=A|A≥A|⊥
```

```
spec(f) :  
∀xy.f(x,y)=f(y,x)+f(0,1)
```

SMT Solver
(cvc5)

[Reynolds et al CAV 2015]

Solution
Enumerator

Solution
Verifier

Using an SMT Solver (cvc5) to *Improve Itself*

1. Rewrite Rule Synthesis

$$\exists t_1 t_2. \forall x. t_1[x] = t_2[x], \quad t_1 \not\rightarrow t_2$$

[Noetzli et al SAT 2019]

2. Semantics-guided test case generation

$$\exists Q. \exists_{\leq n} x \in S. Q(x)$$

3. Solving Quantified Bit-Vectors (and Floating Points) Using Invertibility Conditions

$$\exists IC. \forall st. IC(s, t) \Leftrightarrow \exists x. x \oplus s \sim t$$

[Niemetz et al CAV 2018,
Brain et al CAV 2019]

...can tackle these problems using syntax-guided synthesis

Application #1: Rewrite Rule Synthesis

Rewriting is Important for SMT Solving

- SMT solvers use a “**rewriter**” to put constraints in some normal form
 - E.g. $x+0 \rightarrow x$, $x-y \rightarrow x + (-1 * y)$, $x=x-2 \rightarrow \perp$
- Having a good rewriter is highly **critical to performance**
 - In particular, theory of bit-vectors, strings, floating points
 - Single rewrite may make problem go from hard → trivial

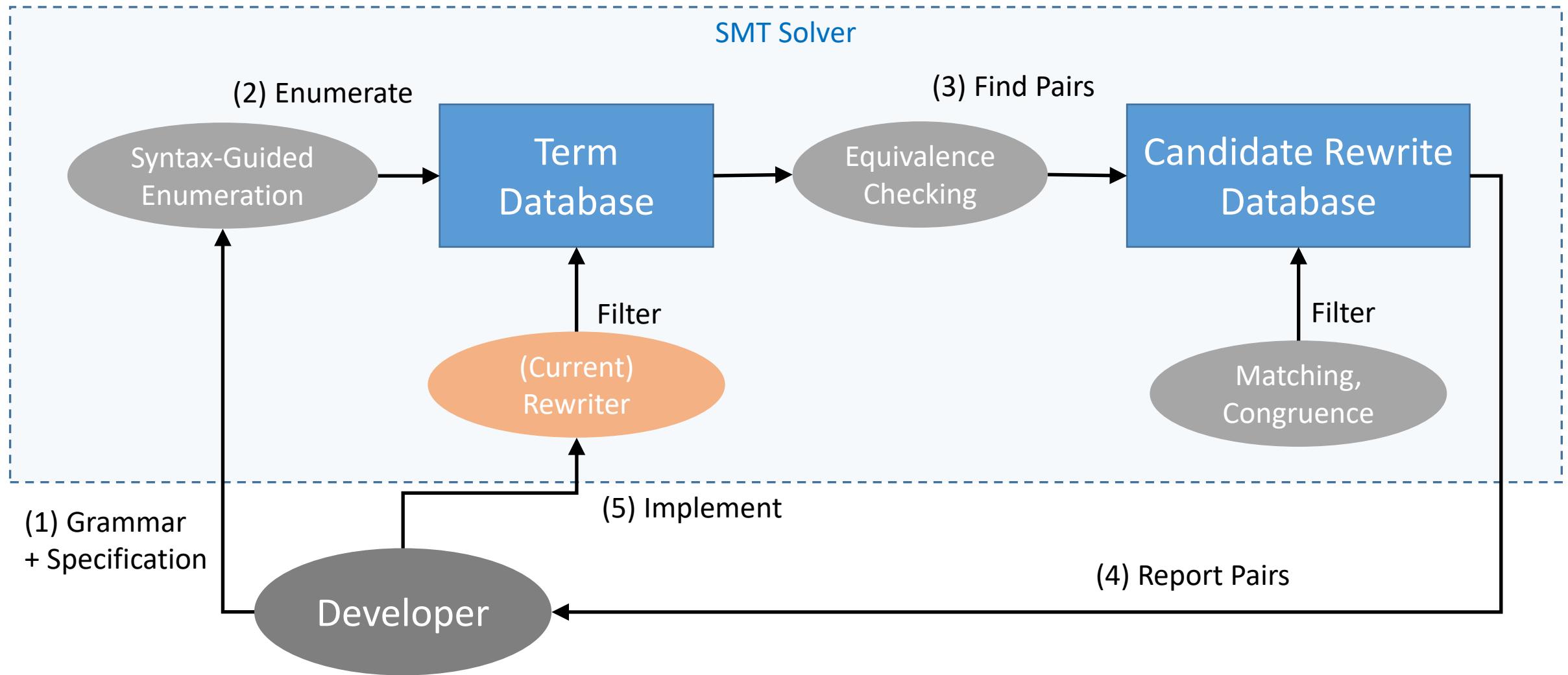
Rewrite Rules are *Difficult to Implement*

- Hard to find **commonly applicable rewrites**
 - Analyze problem instances, solver runs
- What rewrites have I not **already implemented?**
- Time consuming, **many lines of code**
 - cvc5's BV rewriter ~3500 LOC
 - cvc5's string rewriter >5000 LOC

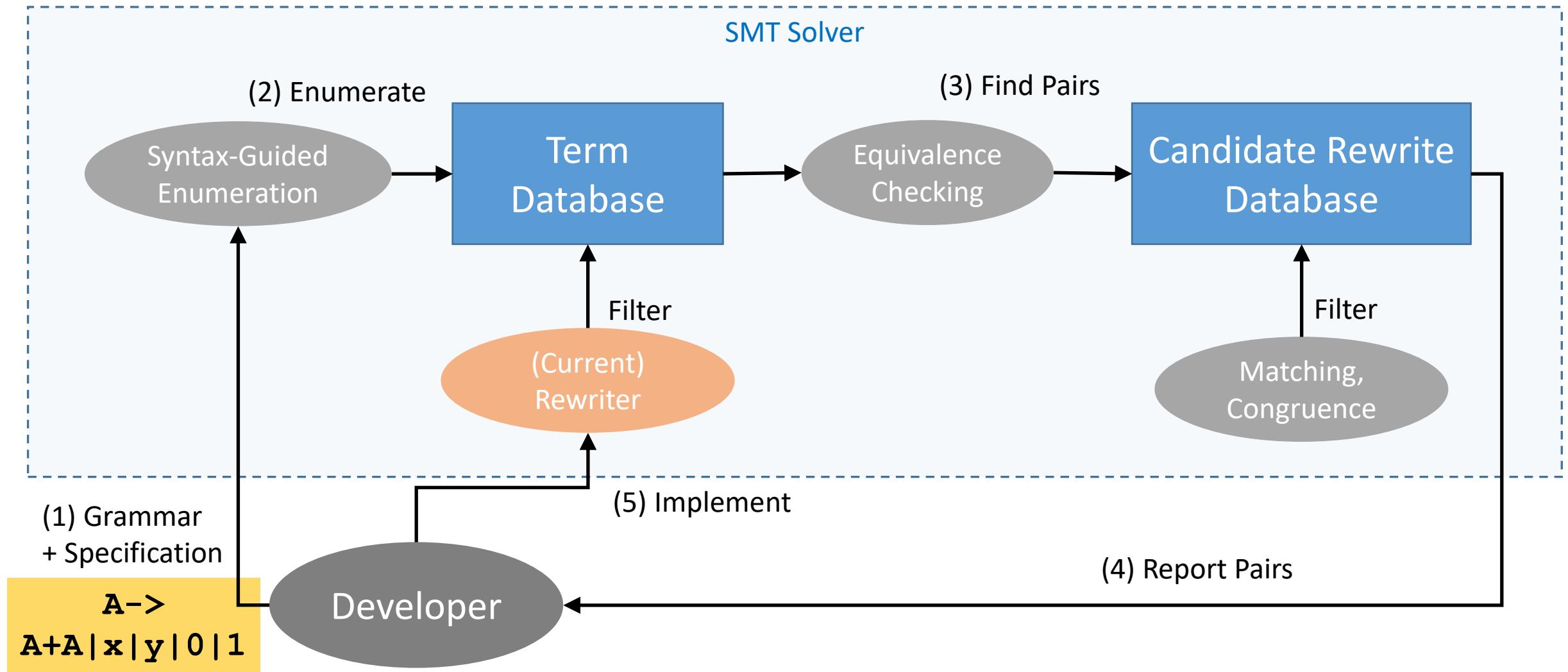
Rewrite Rule Synthesis

- Use the **syntax-guided enumeration** to assist the developer to **implement** the solver's **rewriter**
 - ⇒ Increase **productivity** of the developer
 - ⇒ Increase **confidence** in the correctness of the rewriter

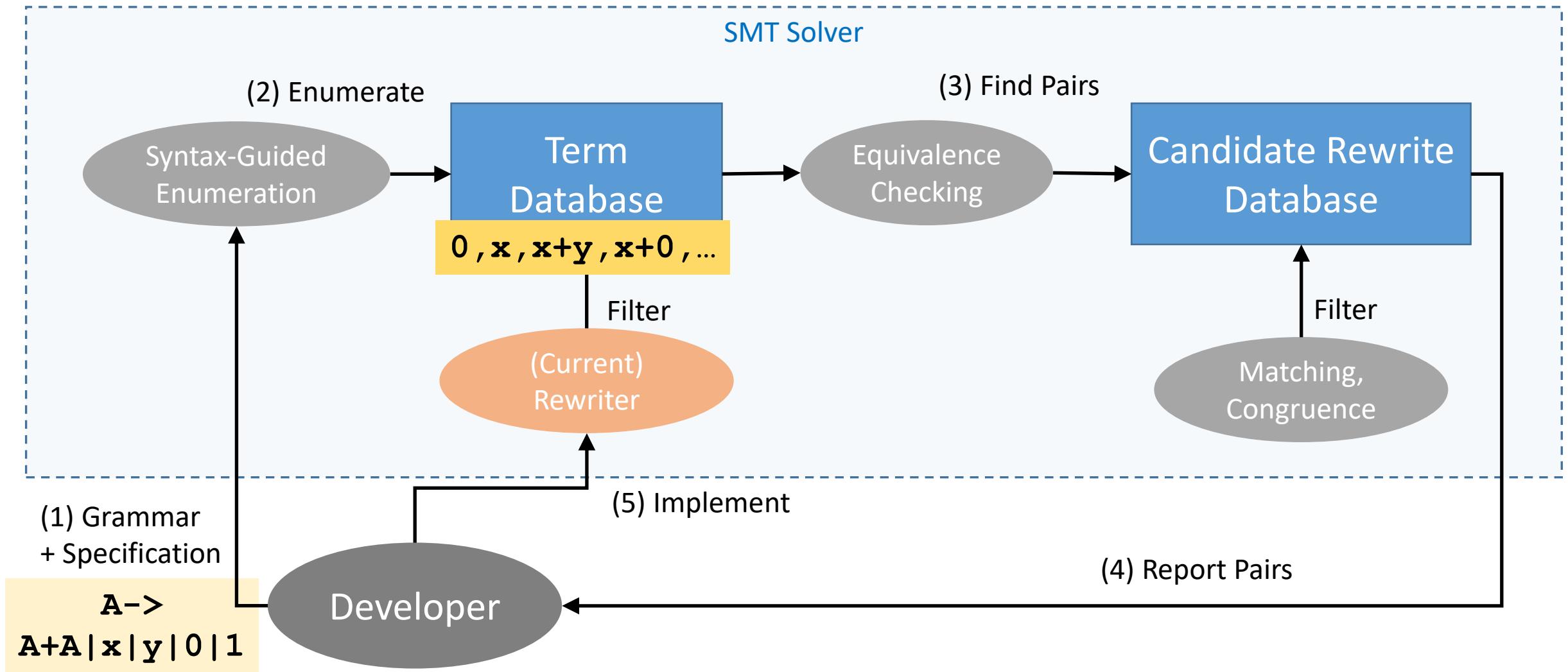
(Partially) Automated Rewrite Rule Generation



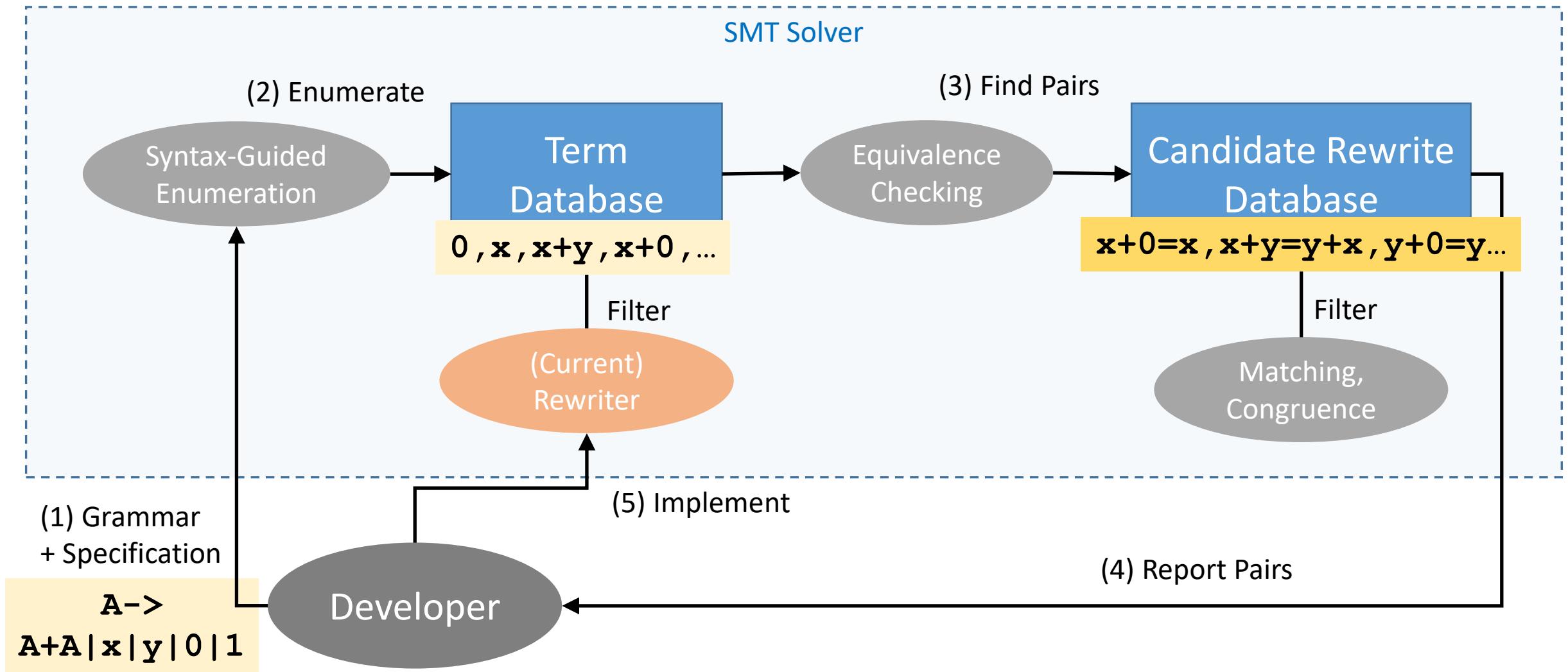
(Partially) Automated Rewrite Rule Generation



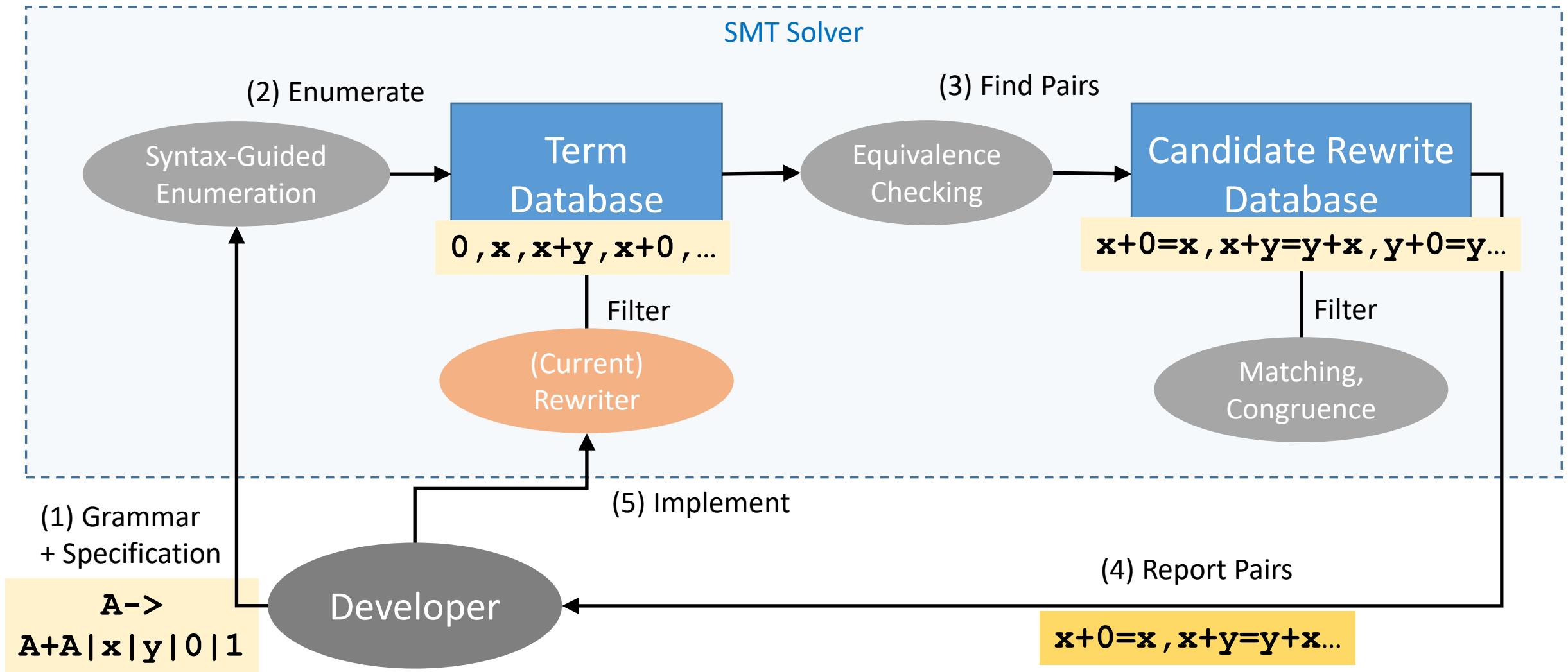
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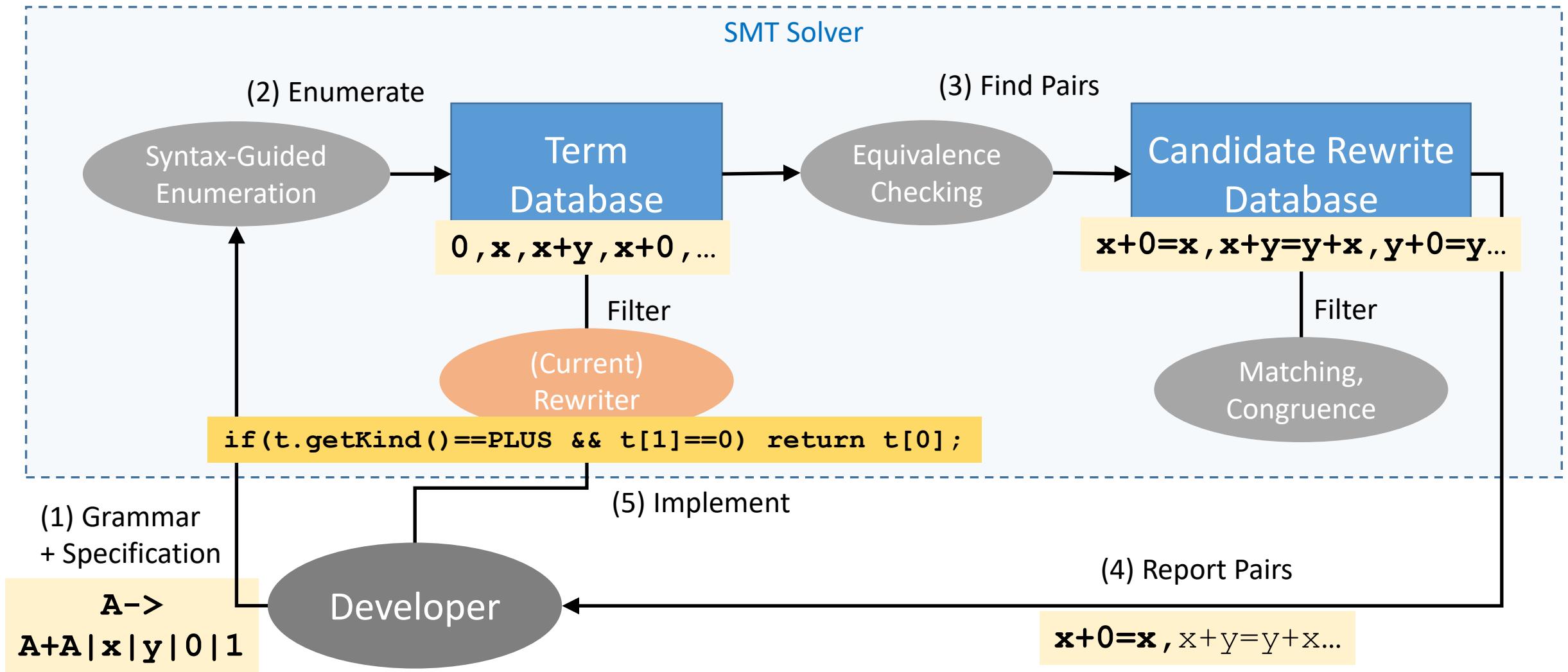
(Partially) Automated Rewrite Rule Generation



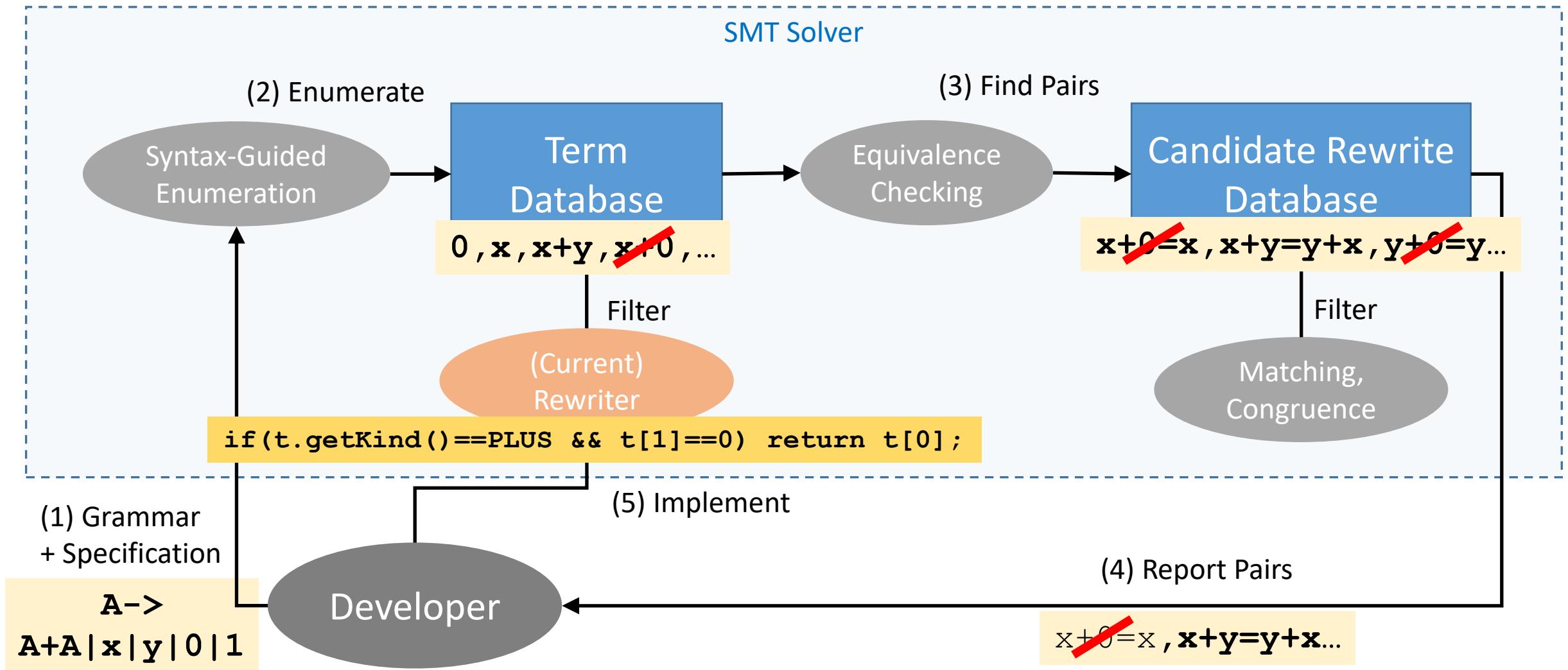
(Partially) Automated Rewrite Rule Generation



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(Partially) Automated Rewrite Rule Generation

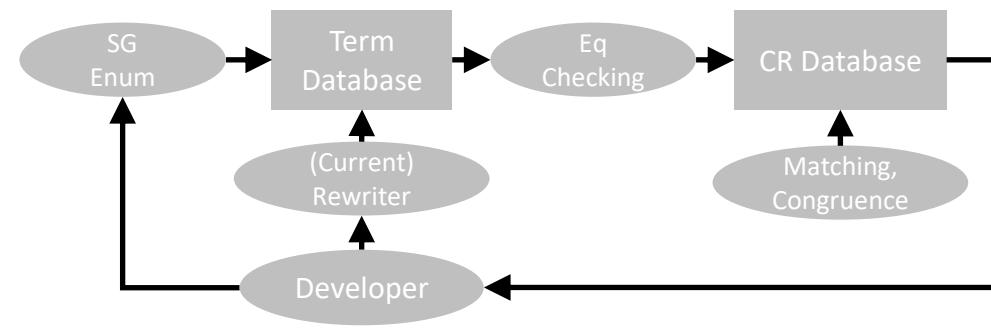


Experience

```
(synth-fun f
  ((x String) (y String) (z Int))
  String (
    (Start String (
      x y "A" "B" ""
      (str.++ Start Start)
      (str.replace Start Start Start)
      (str.at Start ie)
      (int.to.str ie)
      (str.substr Start ie ie)))
    (ie Int (
      0 1 z
      (+ ie ie)
      (- ie ie)
      (str.len Start)
      (str.to.int Start)
      (str.indexof Start Start ie)))))
```

```
(synth-fun f ((s (BitVec 4)) (t (BitVec 4)))
  (BitVec 4) (
    (Start (BitVec 4) (
      s t #x0
      (bvneg Start)
      (bvnot Start)
      (bvadd Start Start)
      (bvmul Start Start)
      (bvand Start Start)
      (bvlshr Start Start)
      (bvor Start Start)
      (bvshl Start Start))))))
```

```
(synth-fun f
  ((x Bool) (y Bool)
   (z Bool) (w Bool))
  Bool (
    (Start Bool (
      (and d1 d1) (not d1)
      (or d1 d1) (xor d1 d1)))
    (d1 Bool (
      x (and d2 d2) (not d2)
      (or d2 d2) (xor d2 d2)))
    (d2 Bool (
      w (and d3 d3) (not d3)
      (or d3 d3) (xor d3 d3)))
    (d3 Bool (
      y (and d4 d4) (not d4)
      (or d4 d4) (xor d4 d4)))
    (d4 Bool (z))))
```



Examples of Rewrites

- Bit-Vectors

$$\begin{aligned} \text{bvlshr}(x, x) &\rightarrow \#x0000 \\ x+1 &\rightarrow \sim(-x) \end{aligned}$$

$$\begin{aligned} x - (x \& y) &\rightarrow x \& \sim y \\ (x \& y) + (x \mid y) &\rightarrow x+y \end{aligned}$$

$$\begin{aligned} \text{concat}(\#x1, x) = \text{concat}(\#x0, y) &\rightarrow \perp \\ \text{bvxor}(x, x \& y) &\rightarrow \sim y \& x \end{aligned}$$

- Strings

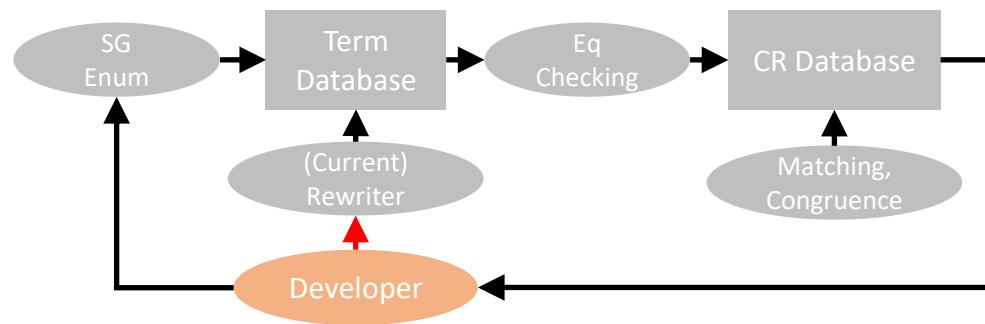
$$\begin{aligned} x++"A" = "B"++x &\rightarrow \perp \\ \text{contains}(x, x++"A") &\rightarrow \perp \\ "A"++x = "A"++y &\rightarrow x=y \end{aligned}$$

$$\begin{aligned} \text{indexof}("ABCDE", x, 3) &\rightarrow \text{indexof}("AAADE", x, 3) \\ \text{replace}(x, x++y, y) &\rightarrow \text{replace}(x, x++y, "") \\ \text{contains}("ABCD", "C"++x++"B") &\rightarrow \perp \end{aligned}$$

- Booleans

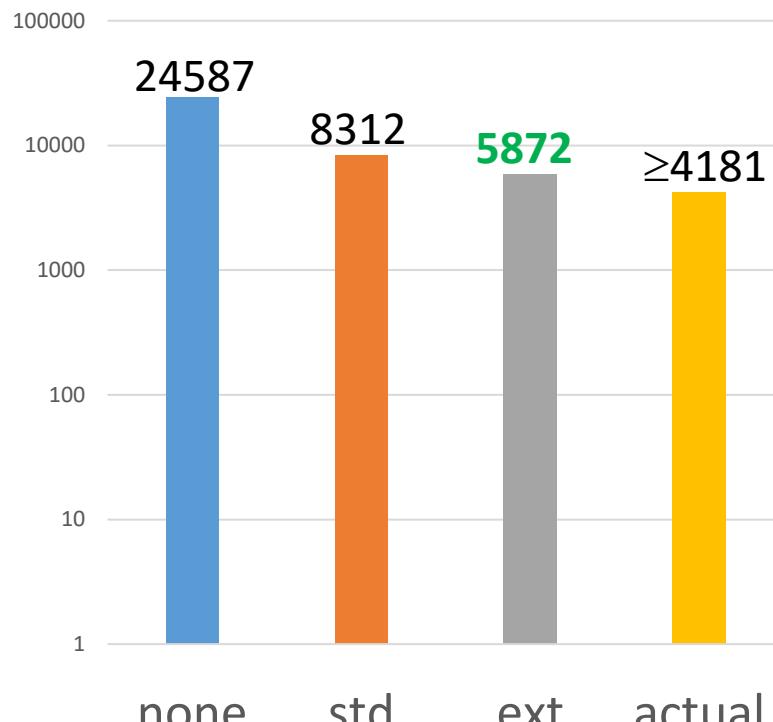
$$\begin{aligned} A \wedge (A \vee B) &\rightarrow A \wedge B \\ A = A \& B &\rightarrow \neg A \vee B \end{aligned}$$

$$\begin{aligned} (A \vee C) \wedge (A \vee B) &\rightarrow A \wedge (C \vee B) \\ (A \vee B) = (A \vee B \vee C) &\rightarrow A \vee B \vee \neg C \end{aligned}$$



Statistics: cvc5's Rewriter (circa 2019):

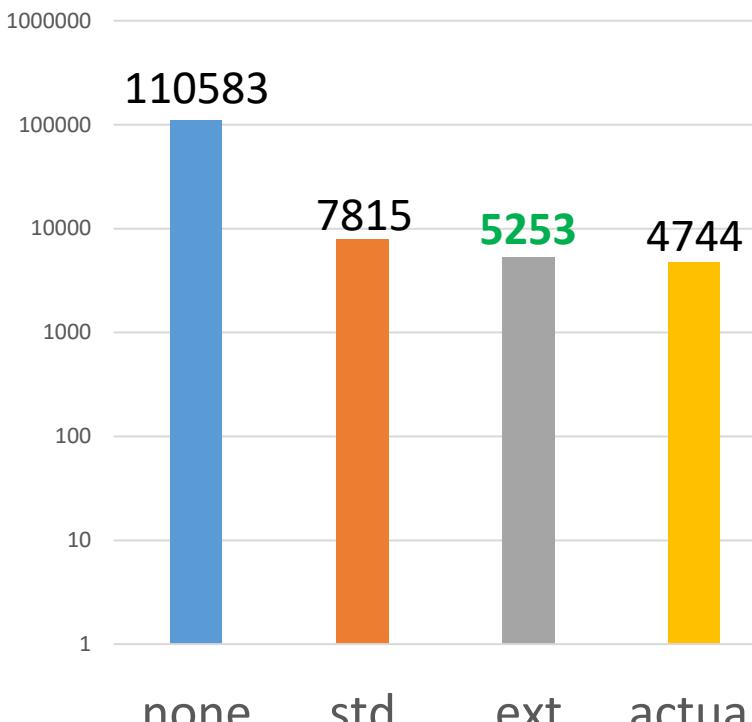
string-term, depth 2



%redundant:
time to
enumerate:

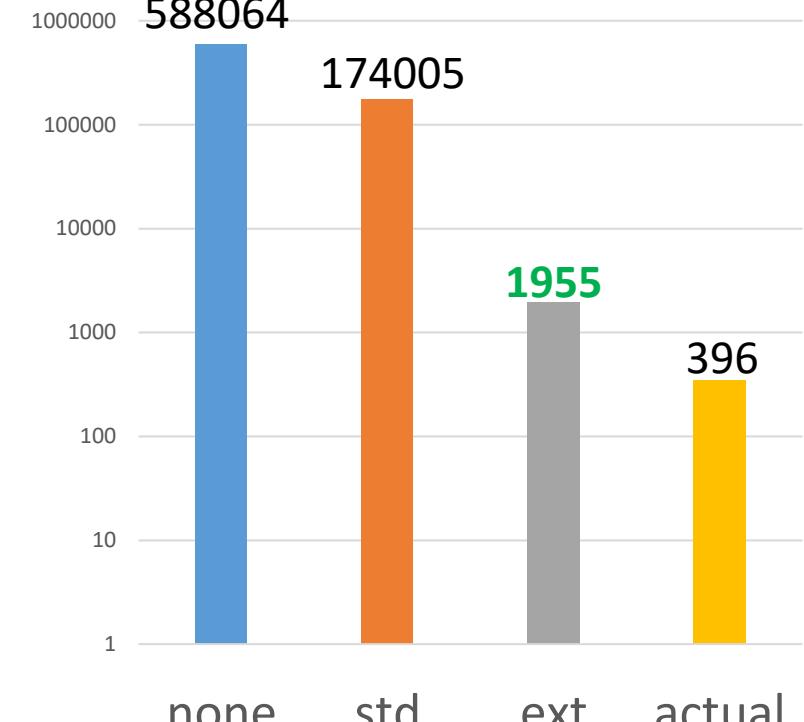
49.7% **28.8%**
90.0 **60.8**

bv-term, depth 3



39.3% **9.7%**
96.4 **55.4**

bool-crci, depth 7



99.8% **82.2%**
19128.8 **60.6**

Impact of Aggressive Simplification *for Strings*

Set		all	-arith	-contain	-msets	z3	OSTRICH
CMU	sat	7947	7746	7948	7946	4585	
	unsat	66	31	66	66	52	
	×	173	409	172	174	3549	
TERMEQ	sat	10	10	10	10	1	
	unsat	49	36	27	49	36	
	×	22	35	44	22	44	
SLOG	sat	1302	1302	1302	1302	1100	1289
	unsat	2082	2082	2082	2082	2075	2082
	×	7	7	7	7	216	20
APLAS	sat	132	132	132	132	10	
	unsat	292	291	171	171	94	
	×	159	160	280	280	479	
Total	sat	9391	9190	9392	9390	5696	1289
	unsat	2489	2440	2346	2368	2257	2082
	×	361	611	503	483	4288	8870

[Reynolds/Noetzli/Tinelli/Barrett CAV 19]

- arith: w/o arithmetic simplifications
- contain: w/o contain-based simplifications
- mset: w/o multiset-based simplifications

- cvc5 uses >5000 lines of C++ for simplification rules (and growing)
 - Important aspect of modern string solving

Application #2: Improving Confidence in the SMT Solver

Improving Confidence: Rewriting

- *Does my SMT solver implement any unsound rewrites?*

Improving Confidence: Rewriting

Grammar of interest

```
(synth-fun f ((s BV8) (t BV8)) BV8
  ((Start BV8
    (s t #x00 #x01
      ~Start
      -Start
      bvlshr(Start Start)
      Start & Start
      Start + Start
    )) )
```

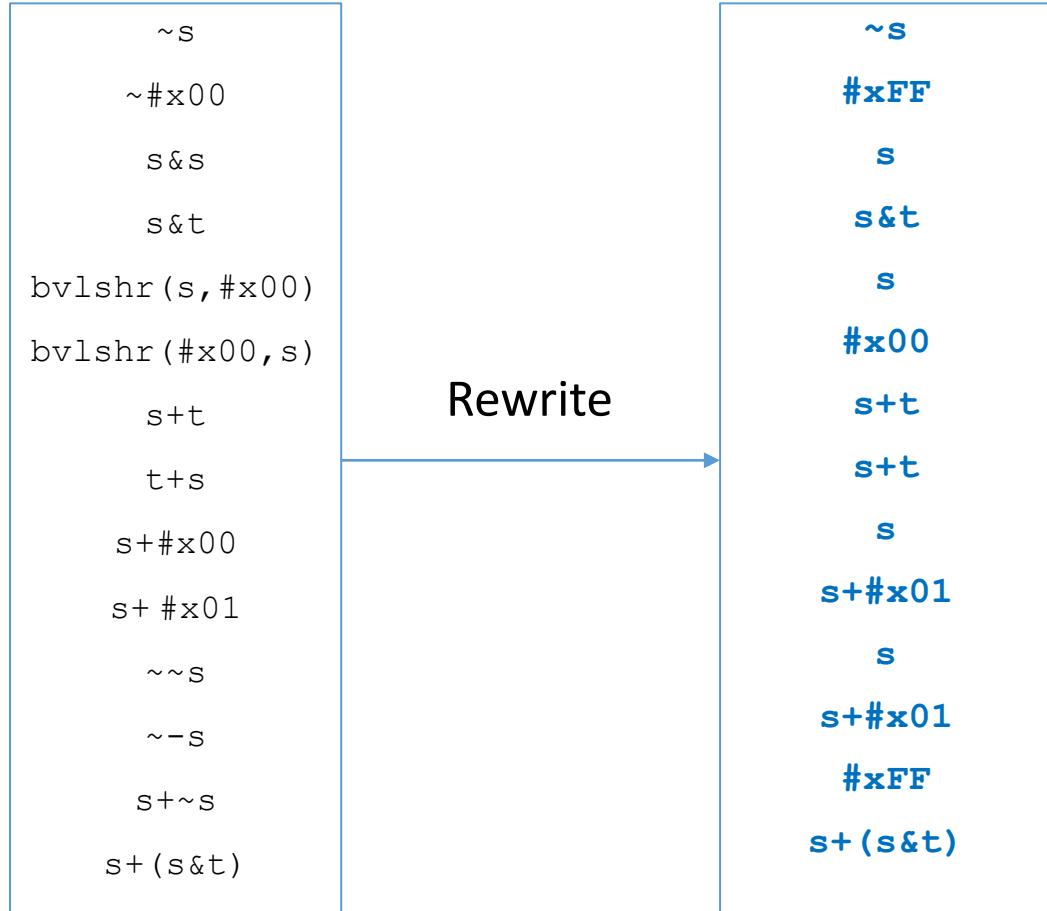
Improving Confidence: Rewriting

```
~s  
~#x00  
s&s  
s&t  
bvlshr(s,#x00)  
bvlshr(#x00,s)  
s+t  
t+s  
s+#x00  
s+ #x01  
~~s  
~-s  
s+~s  
s+(s&t)
```

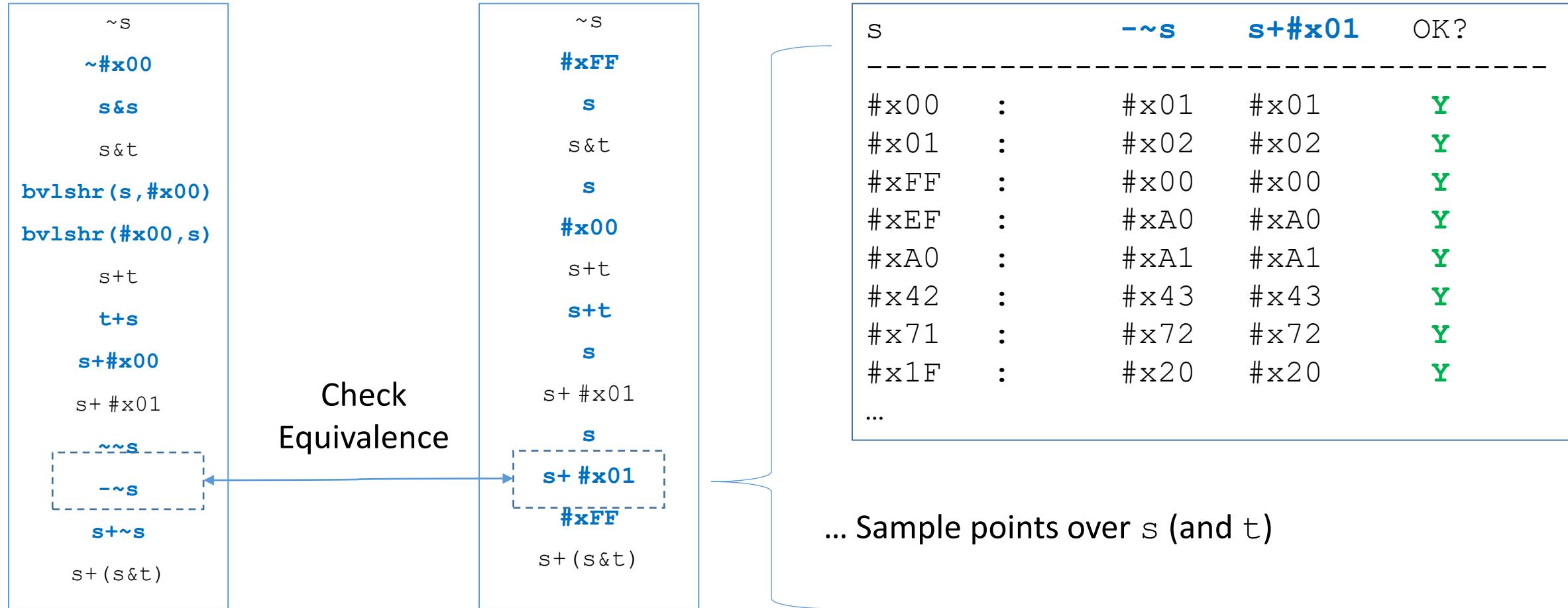
Syntax-Guided Term Enumeration

```
(synth-fun f ((s BV8) (t BV8)) BV8  
  ((Start BV8  
    (s t #x00 #x01  
     ~Start  
     -Start  
     bvlshr(Start Start)  
     Start & Start  
     Start + Start  
   )))
```

Improving Confidence: Rewriting



Improving Confidence: Rewriting



Improving Confidence: Rewriting

⇒ Has been critical for *finding bugs* in newly written rewriter code

```
(unsound-rewrite (bvuge (bvadd x #x0001) x) true)
; --sygus-rr-verify detected unsoundness in the rewriter!
; Terms have the same rewritten form but are not equivalent
; for x=#xFFFF, where they evaluate to:
; (bvuge (bvadd x #x0001) x) = false
; true = true
```

⇒ Run as part of cvc5's regression tests:

CVC4 / CVC4

Watch 33 Unstar 280 Fork 98

Code Issues 237 Pull requests 31 Projects 1 Wiki Insights

Add tests that enumerate and verify rewrite rules #2344 Edit

Merged ajreynol merged 5 commits into cvc4:master from 4tXJ7f:addVerifyTests on Aug 24, 2018

Conversation 3 Commits 5 Checks 0 Files changed 9 +146 -21

4tXJ7f commented on Aug 20, 2018 • edited

The regression script now avoids running with `--check-synth-sol` when `--sygus-rr` is used.

Reviewers ajreynol

Assignees ajreynol

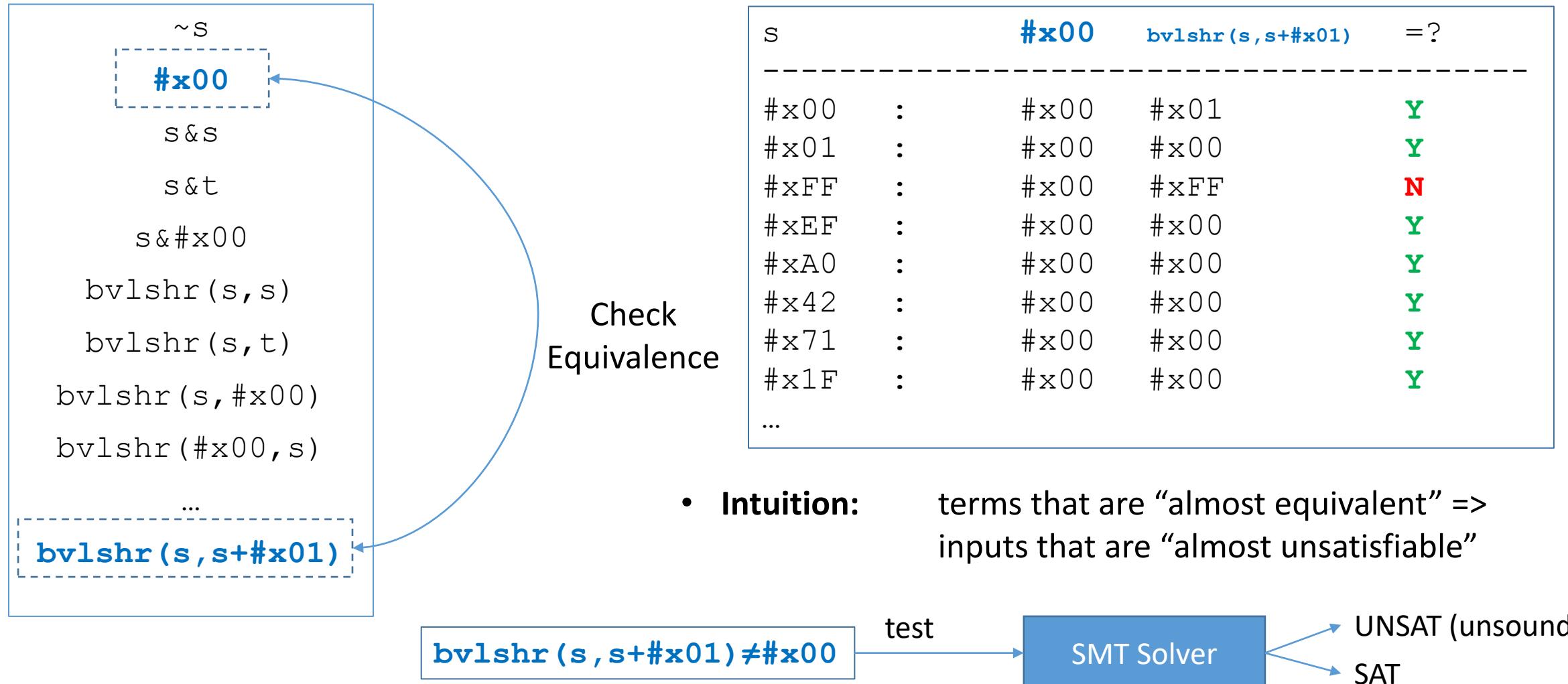
Add tests that enumerate and verify rewrite rules ... Verified 272899c

Improving Confidence: Query Generation

```
~s  
#x00  
s&s  
s&t  
s&#x00  
bvlshr(s,s)  
bvlshr(s,t)  
bvlshr(s,#x00)  
bvlshr(#x00,s)  
...  
bvlshr(s,s+#x01)
```

Syntax-Guided Term Enumeration

Improving Confidence: Query Generation



Application #3: Solving Quantified Inputs via Invertibility Conditions

Solving Quantified Bit-Vectors: Example

- Consider quantifier elimination problem for bit-vectors:

$$\exists x : \text{BV}_8 . s * x = t \Leftrightarrow ???$$

⇒ Applications in proving safety properties, compiler optimizations

- Common solving technique is model-based instantiation [Wintersteiger et al 2013]
 - Based on *values*: above is equivalent $s * \#x00 = t \vee s * \#x01 = t \vee s * \#x02 = t \vee \dots$
 - Scalability issues for larger bit-widths
- Idea:** Use SyGuS to find *invertibility conditions* for bit-vector equations
⇒ Compact form for quantifier elimination

What is an Invertibility Condition?

- Some equations are “invertible”, e.g.:
 - $s + \textcolor{red}{x} = t$... always has solution $\textcolor{red}{x} = t - s$
- Some equations are not, e.g.:
 - $s * \textcolor{red}{x} = t$... x has *no solution* when, e.g. $s=2, t=3$

What is an Invertibility Condition?

- $s + \textcolor{red}{x} = t$... always has solution $\textcolor{red}{x} = t - s$
- $s^* \textcolor{red}{x} = t$... x has *no solution* when, e.g. $s=2, t=3$
- **Challenge:** it is possible to characterize exactly when x has a solution?
 - Find a predicate $\text{IC}(s, t)$ such that x has a solution iff $\text{IC}(s, t)$ is satisfiable
 - We call IC an “invertibility condition”
 - Invertibility Conditions \Rightarrow QE procedure for “linear” formulas

What is an Invertibility Condition?

- For terms s, t , operator \oplus and relation \sim
 - An *invertibility condition* $IC(s, t)$ is a quantifier-free formula such that:

$$\exists x. (x \oplus s \sim t) \Leftrightarrow IC(s, t)$$

is T-valid.

Finding Invertibility Conditions for BV

$$\exists x . (x \oplus s \sim t) \Leftrightarrow IC(s, t)$$

- Applied to theory of Bit-Vectors [Niemetz et al CAV 2018]
- Signature of BV has 15 operators, 4 relations ($=/\neq$, signed/unsigned inequality)
⇒ Total of 162 invertibility conditions to find
- Some took several hours to find by hand ∴ *use SyGuS*
 - Using SyGuS, found **118** of **162** conditions
 - Many simpler than hand-crafted ones
 - When combined with hand-crafted ICs, found all **162** conditions

Invertibility Conditions for BV

$\ell[x]$	\approx	$\not\approx$
$x \cdot s \bowtie t$	$(-s \mid s) \& t \approx t$	$s \not\approx 0 \vee t \not\approx 0$
$x \bmod s \bowtie t$	$\sim(-s) \geq_u t$	$s \not\approx 1 \vee t \not\approx 0$
$s \bmod x \bowtie t$	$(t + t - s) \& s \geq_u t$	$s \not\approx 0 \vee t \not\approx 0$
$x \div s \bowtie t$	$(s \cdot t) \div s \approx t$	$s \not\approx 0 \vee t \not\approx \sim 0$
$s \div x \bowtie t$	$s \div (s \div t) \approx t$	$\begin{cases} s \& t \approx 0 & \text{for } \kappa(s) = 1 \\ \top & \text{otherwise} \end{cases}$
$x \& s \bowtie t$	$t \& s \approx t$	$s \not\approx 0 \vee t \not\approx 0$
$x \mid s \bowtie t$	$t \mid s \approx t$	$s \not\approx \sim 0 \vee t \not\approx \sim 0$
$x \gg s \bowtie t$	$(t \ll s) \gg s \approx t$	$t \not\approx 0 \vee s <_u \kappa(s)$
$s \gg x \bowtie t$	$\bigvee_{i=0}^{\kappa(s)} s \gg i \approx t$	$s \not\approx 0 \vee t \not\approx 0$
$x \gg_a s \bowtie t$	$(s <_u \kappa(s) \Rightarrow (t \ll s) \gg_a s \approx t) \wedge (s \geq_u \kappa(s) \Rightarrow (t \approx \sim 0 \vee t \approx 0))$	\top
$s \gg_a x \bowtie t$	$\bigvee_{i=0}^{\kappa(s)} s \gg_a i \approx t$	$(t \not\approx 0 \vee s \not\approx 0) \wedge (t \not\approx \sim 0 \vee s \not\approx \sim 0)$
$x \ll s \bowtie t$	$(t \gg s) \ll s \approx t$	$t \not\approx 0 \vee s <_u \kappa(s)$
$s \ll x \bowtie t$	$\bigvee_{i=0}^{\kappa(s)} s \ll i \approx t$	$s \not\approx 0 \vee t \not\approx 0$
$x \circ s \bowtie t$	$s \approx t[\kappa(s) - 1 : 0]$	\top
$s \circ x \bowtie t$	$s \approx t[\kappa(t) - 1 : \kappa(t) - \kappa(s)]$	\top

} ICs for $=, \neq$

...not pictured:
ICs for $\text{bvuge}, \text{bvugt},$
 $\text{bvsge}, \text{bvsigt}$

Table 2. Conditions for the invertibility of bit-vector operators over (dis)equality. Those for \cdot , $\&$ and \mid are given modulo commutativity of those operators.

Invertibility Conditions for BV

$\ell[x]$	\approx	$\not\approx$
$x \cdot s \bowtie t$	$(-s \mid s) \& t \approx t$	$s \not\approx 0 \vee t \not\approx 0$
$x \bmod s \bowtie t$	$\sim(-s) \geq_u t$	$s \not\approx 1 \vee t \not\approx 0$
$s \bmod x \bowtie t$	$(t + t - s) \& s \geq_u t$	$s \not\approx 0 \vee t \not\approx 0$
$x \div s \bowtie t$	$(s \cdot t) \div s \approx t$	$s \not\approx 0 \vee t \not\approx \sim 0$
$s \div x \bowtie t$	$s \div (s \div t) \approx t$	$\begin{cases} s \& t \approx 0 & \text{for } \kappa(s) = 1 \\ \top & \text{otherwise} \end{cases}$
$x \& s \bowtie t$	$t \& s \approx t$	$s \not\approx 0 \vee t \not\approx 0$
$x \mid s \bowtie t$	$t \mid s \approx t$	$s \not\approx \sim 0 \vee t \not\approx \sim 0$
$x \gg s \bowtie t$	$(t \ll s) \gg s \approx t$	$t \not\approx 0 \vee s <_u \kappa(s)$
$s \gg x \bowtie t$	$\bigvee_{i=0}^{\kappa(s)} s \gg i \approx t$	$s \not\approx 0 \vee t \not\approx 0$
$x \gg_a s \bowtie t$	$(s <_u \kappa(s) \Rightarrow (t \ll s) \gg_a s \approx t) \wedge (s \geq_u \kappa(s) \Rightarrow (t \approx \sim 0 \vee t \approx 0))$	\top
$s \gg_a x \bowtie t$	$\bigvee_{i=0}^{\kappa(s)} s \gg_a i \approx t$	$(t \not\approx 0 \vee s \not\approx 0) \wedge (t \not\approx \sim 0 \vee s \not\approx \sim 0)$
$x \ll s \bowtie t$	$(t \gg s) \ll s \approx t$	$t \not\approx 0 \vee s <_u \kappa(s)$
$s \ll x \bowtie t$	$\bigvee_{i=0}^{\kappa(s)} s \ll i \approx t$	$s \not\approx 0 \vee t \not\approx 0$
$x \circ s \bowtie t$	$s \approx t[\kappa(s) - 1 : 0]$	\top
$s \circ x \bowtie t$	$s \approx t[\kappa(t) - 1 : \kappa(t) - \kappa(s)]$	\top

$$\exists x . s^* x = t \iff (-s \mid s) \& t = t$$

- Condition above encodes
"s has fewer trailing zeroes than t"
- Conditions like this one are concise, subtle
 \Rightarrow Excellent target for SyGuS

Table 2. Conditions for the invertibility of bit-vector operators over (dis)equality. Those for \cdot , $\&$ and \mid are given modulo commutativity of those operators.

Experimental Results

- Quantifier Instantiation based on Invertibility Conditions in CVC4
- Won quantified bit-vector (BV) category of SMT-COMP 2018

unsat	Boolector	CVC4	Q3B	Z3	cegqi _m	cegqi _k	cegqi _s	cegqi _b
h-uauto	14	12	93	24	10	103	105	106
keymaera	3917	3790	3781	3923	3803	3798	3888	3918
psyco	62	62	49	62	62	39	62	61
scholl	57	36	13	67	36	27	36	35
tptp	55	52	56	56	56	56	56	56
uauto	137	72	131	137	72	72	135	137
ws-fixpoint	74	71	75	74	75	74	75	75
ws-ranking	16	8	18	19	15	11	12	11
Total unsat	4332	4103	4216	4362	4129	4180	4369	4399
sat	Boolector	CVC4	Q3B	Z3	cegqi _m	cegqi _k	cegqi _s	cegqi _b
h-uauto	15	10	17	13	16	17	16	17
keymaera	108	21	24	108	20	13	36	75
psyco	131	132	50	131	132	60	132	129
scholl	232	160	201	204	203	188	208	211
tptp	17	17	17	17	17	17	17	17
uauto	14	14	15	16	14	14	14	14
ws-fixpoint	45	49	54	36	45	51	49	50
ws-ranking	19	15	37	33	33	31	31	32
Total sat	581	418	415	558	480	391	503	545
Total (5151)	4913	4521	4631	4920	4609	4571	4872	4944

Table 4. Results on satisfiable and unsatisfiable benchmarks with a 300 second timeout.

Invertibility Conditions for Floating Points

- Say I want to find invertibility condition for *floating point* equation:

$$\exists x : FP_{e,s} \cdot x \oplus s \sim t$$

- Can we apply the same approach to Floating Points?
 - ...will it scale?

Invertibility Conditions for Floating Points

$\exists \text{IC}.$ $\forall st : FP_{e,s}.$ $(\exists x : FP_{e,s}. x \oplus s \sim t) \Leftrightarrow \text{IC}(s, t)$

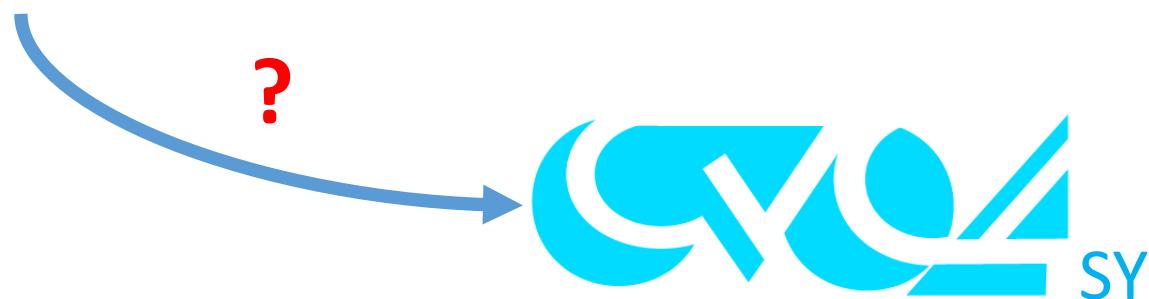


- Can express as a synthesis problem:

...there exists a predicate **IC** that is equivalent to $\exists x : FP_{e,s}. x \oplus s \sim t$

Invertibility Conditions for Floating Points

$$\exists \text{IC}. \forall st : \text{FP}_{e,s}. (\exists x : \text{FP}_{e,s}. x \oplus s \sim t) \Leftrightarrow \text{IC}(s, t)$$



... solve via syntax-guided synthesis (SyGuS)?

How do we find Invertibility Conditions?

$$\exists \text{IC}. \quad \forall s, t : \text{FP}_{\textcolor{red}{e}, \textcolor{red}{s}}. \quad (\exists x : \text{FP}_{\textcolor{red}{e}, \textcolor{red}{s}}. x \oplus s \sim t) \iff \text{IC}(s, t)$$

- **Challenge #1:** problem is parameteric
 - Parameterized by # exponent bits $\textcolor{red}{e}$, # significant bits $\textcolor{red}{s}$

How do we find Invertibility Conditions?

$$\exists \text{IC}. \forall st : \text{FP}_{\color{red}3,5}. (\exists x : \text{FP}_{\color{red}3,5}. x \oplus s \sim t) \Leftrightarrow \text{IC}(s, t)$$

- **Challenge #1:** problem is parameteric
⇒ Solve for a *fixed format*, check if solution generalizes [Niemetz et al CAV 2018]
 - Choose $e=3, s=5$... large enough to exhibit FP behaviors, small enough for synthesis to scale

How do we find Invertibility Conditions?

$$\exists \text{IC}. \ \forall s t : \text{FP}_{3,5}. \ (\exists x : \text{FP}_{3,5} . \ x \oplus s \sim t) \Leftrightarrow \text{IC}(s, t)$$

How do we find Invertibility Conditions?

$$\exists \text{IC}. \quad \forall s t : \text{FP}_{3,5}. \quad (\exists x : \text{FP}_{3,5} . \ x \oplus s \sim t) \iff \text{IC}(s, t)$$

- **Challenge #2:** problem has *three levels* of quantifier alternation
 - ...SyGuS solvers only typically handle two

How do we find Invertibility Conditions?

227

$$\exists \text{IC}. \forall s, t : \text{FP}_{3,5}. \left(\bigvee_{c=1}^{227} c \oplus s \sim t \right) \Leftrightarrow \text{IC}(s, t)$$

- **Challenge #2:** problem has three levels of quantifier alternation
⇒ Expand the **innermost quantifier** [Niemetz et al CAV 2018]
 - Since domain is (relatively) small and finite
 - Only 227 values for $\text{FP}_{3,5}$

How do we find Invertibility Conditions?

227

$$\exists \text{IC}. \forall st : \text{FP}_{3,5}. \left(\bigvee_{c=1} c \oplus s \sim t \right) \Leftrightarrow \text{IC}(s, t)$$

...can now give as input to SyGuS solver

How do we find Invertibility Conditions?

$$\exists \text{IC}. \forall st : \text{FP}_{3,5}. \left(\bigvee_{c=1}^{227} c \oplus s \sim t \right) \Leftrightarrow \text{IC}(s, t)$$



- **Challenge #3: Scalability!**
 - With respect to BV synthesis @ 4 bits [Niemetz et al CAV 2018]:
 - Roughly 14 times more constraints, q.f. FP is much harder than BV

How do we find Invertibility Conditions?

227

$$\exists \text{IC}. \forall st : \text{FP}_{3,5}. \left(\bigvee_{c=1} c \oplus s \sim t \right) \Leftrightarrow \text{IC}(s, t)$$

- **Challenge #3:** Scalability

How do we find Invertibility Conditions?

$$\exists \text{IC. } \underset{s=1}{\overset{227}{\wedge}} \underset{t=1}{\overset{227}{\wedge}} c_{s,t} \Leftrightarrow \text{IC}(s, t)$$

\nwarrow

$$\exists x. x^* s = t ? \text{ where } s, t \text{ are constants}$$

- **Challenge #3:** Scalability

⇒ Statically compute the I/O behavior of *entire domain* of $\text{IC}(s, t)$

- Each $c_{s,t}$ is determined by a quantifier-free satisfiability query
 - $227 * 227 = 51529$, takes ~10 minutes

How do we find Invertibility Conditions?

$$\exists \text{IC. } \bigwedge_{s=1}^{227} \bigwedge_{t=1}^{227} c_{s,t} \Leftrightarrow \text{IC}(s, t)$$

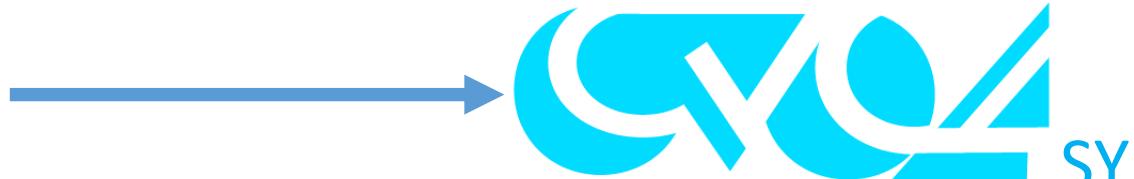
How do we find Invertibility Conditions?

$$\begin{matrix} 227 & 227 \\ \exists \text{IC. } & \wedge \quad \wedge \\ & s=1 \quad t=1 \end{matrix}$$

$c_{s,t} \Leftrightarrow \text{IC}(s,t)$

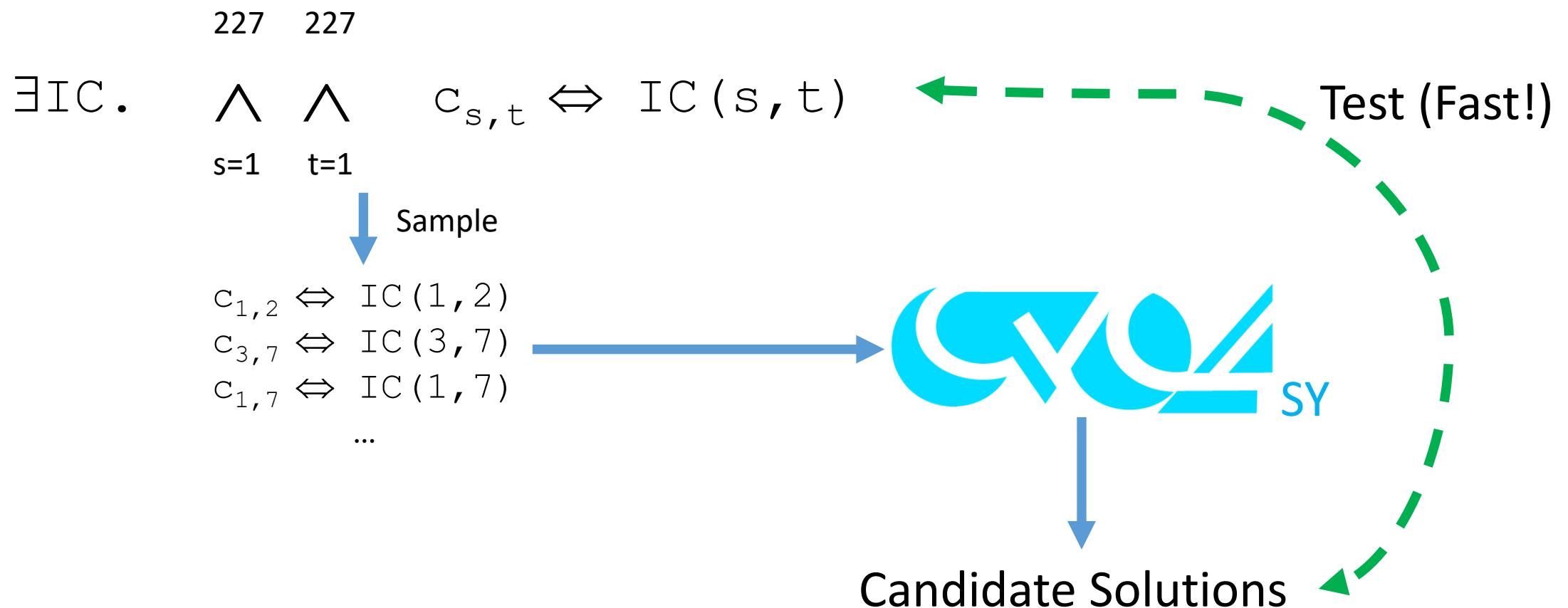
↓ Sample

$$\begin{matrix} c_{1,2} \Leftrightarrow \text{IC}(1,2) \\ c_{3,7} \Leftrightarrow \text{IC}(3,7) \\ c_{1,7} \Leftrightarrow \text{IC}(1,7) \\ \dots \end{matrix}$$

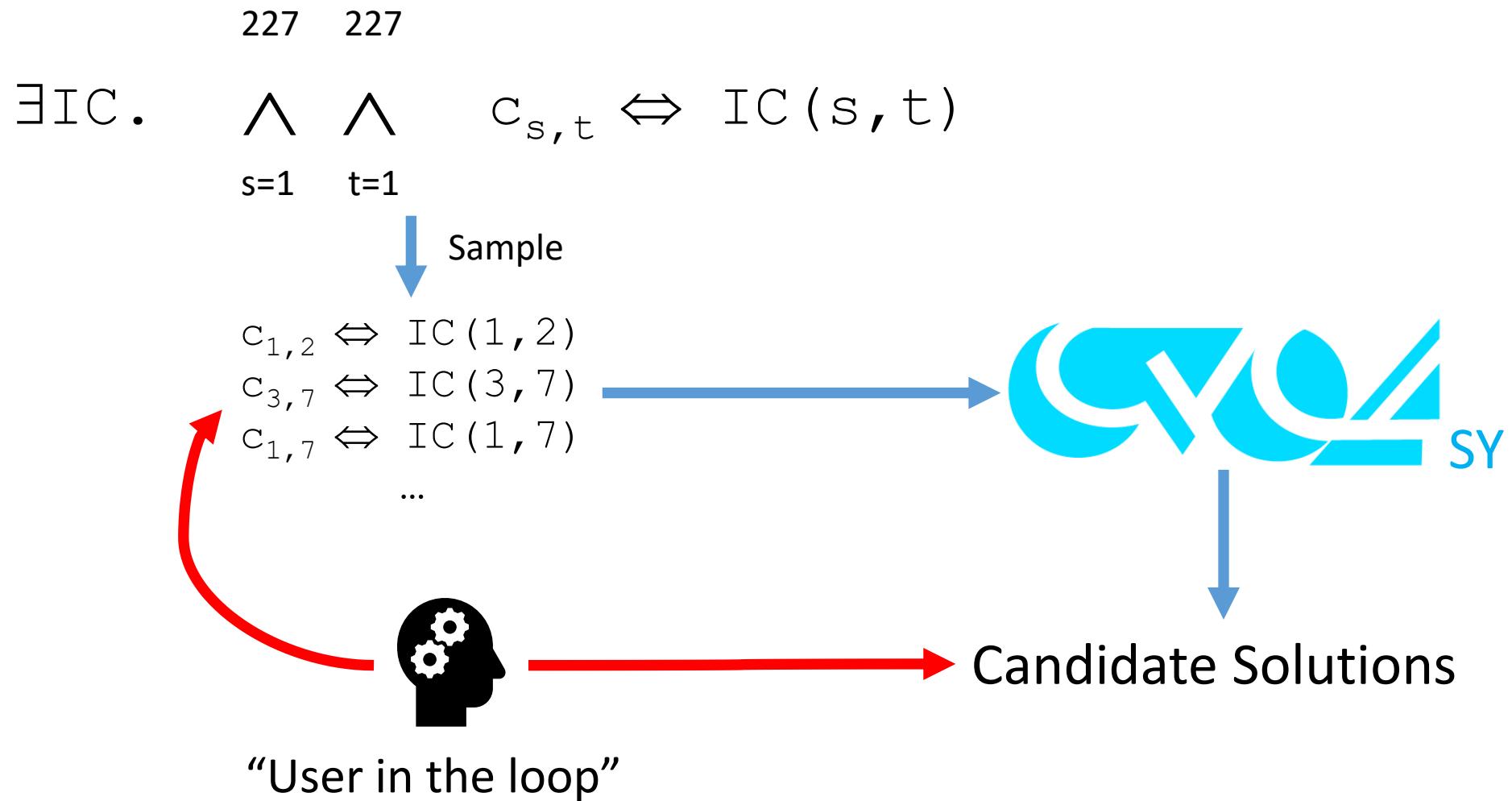


Candidate Solutions

How do we find Invertibility Conditions?

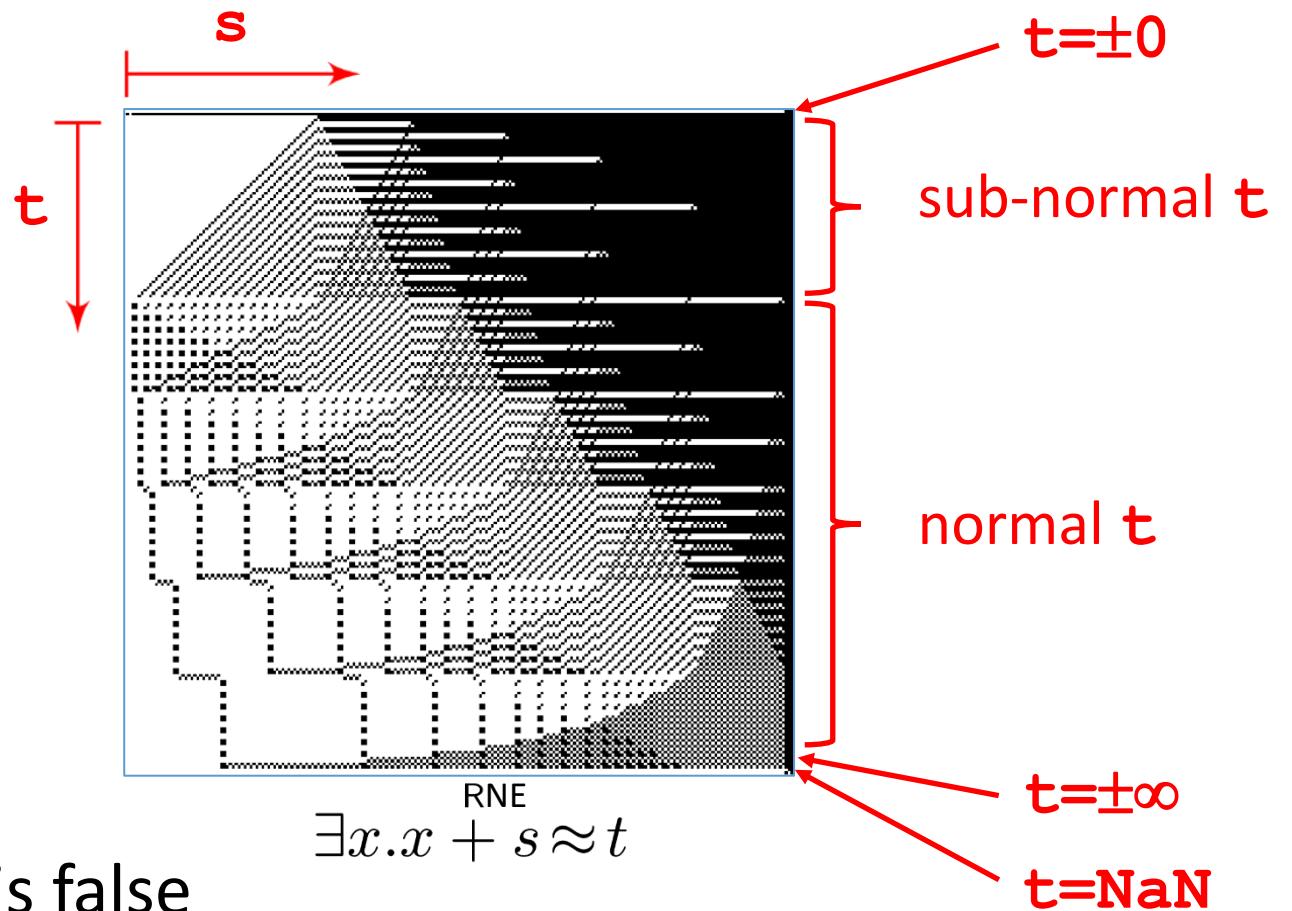


How do we find Invertibility Conditions?



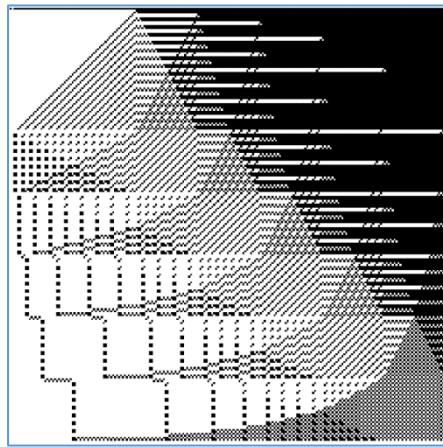
Visualizing I/O Specs of Invertibility Conditions

$$\begin{array}{cc} 227 & 227 \\ \exists \text{IC. } & \wedge \quad \wedge \quad c_{s,t} \Leftrightarrow \text{IC}(s,t) \\ s=1 & t=1 \end{array}$$

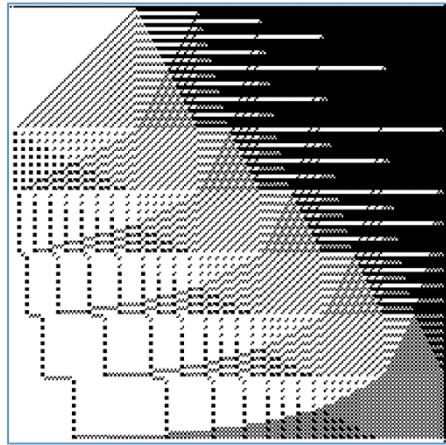


- White = IC is true, Black = IC is false
⇒ Behavior of IC is highly complex!

Synthesizing Invertibility Conditions



Synthesizing Invertibility Conditions

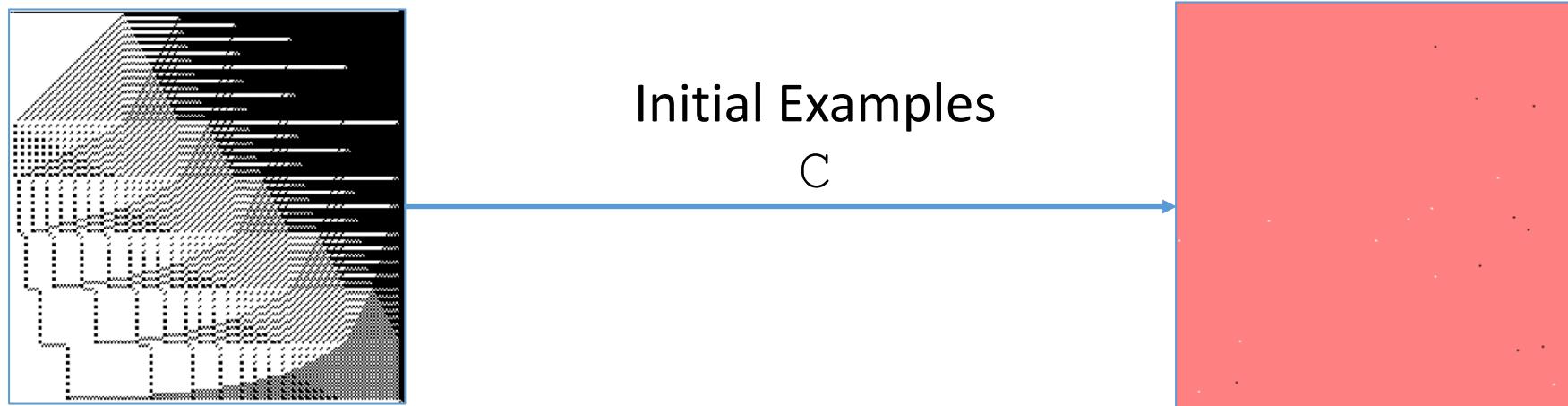


“Full I/O Specification for IC”
(Verifier)

(Synthesizer)



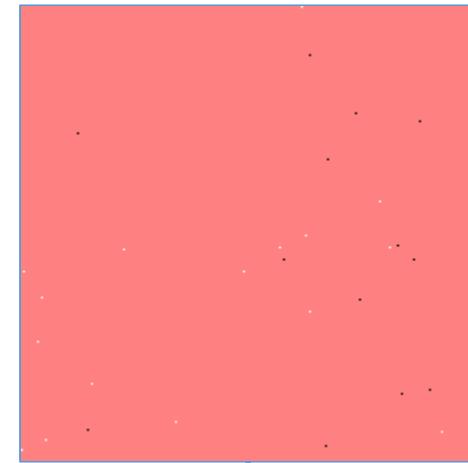
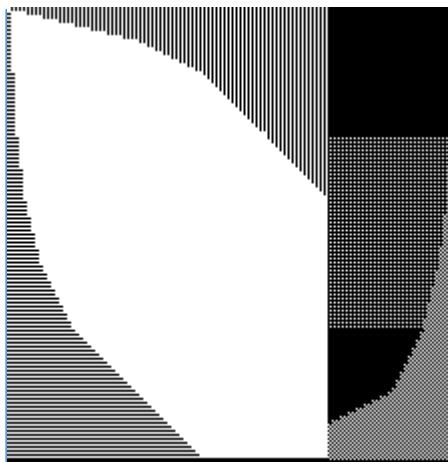
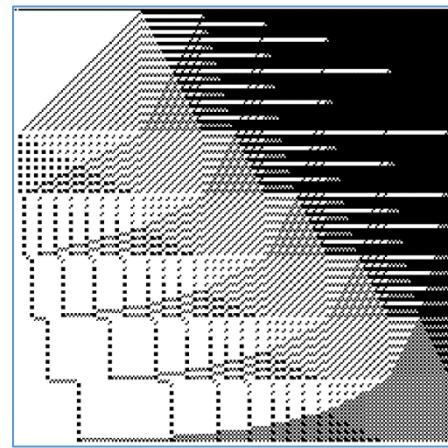
Synthesizing Invertibility Conditions



Red = Counterexample not specified

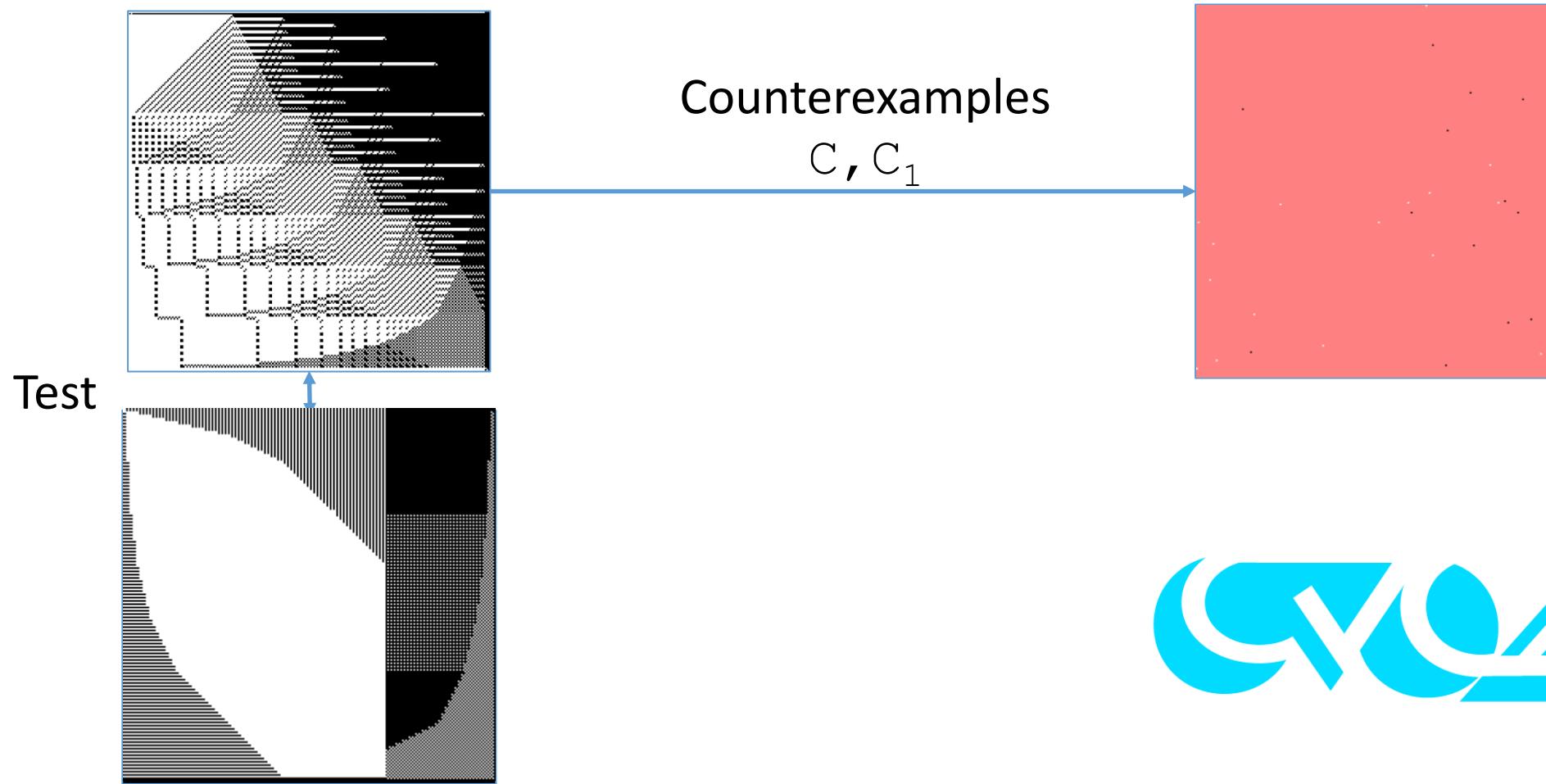


Synthesizing Invertibility Conditions

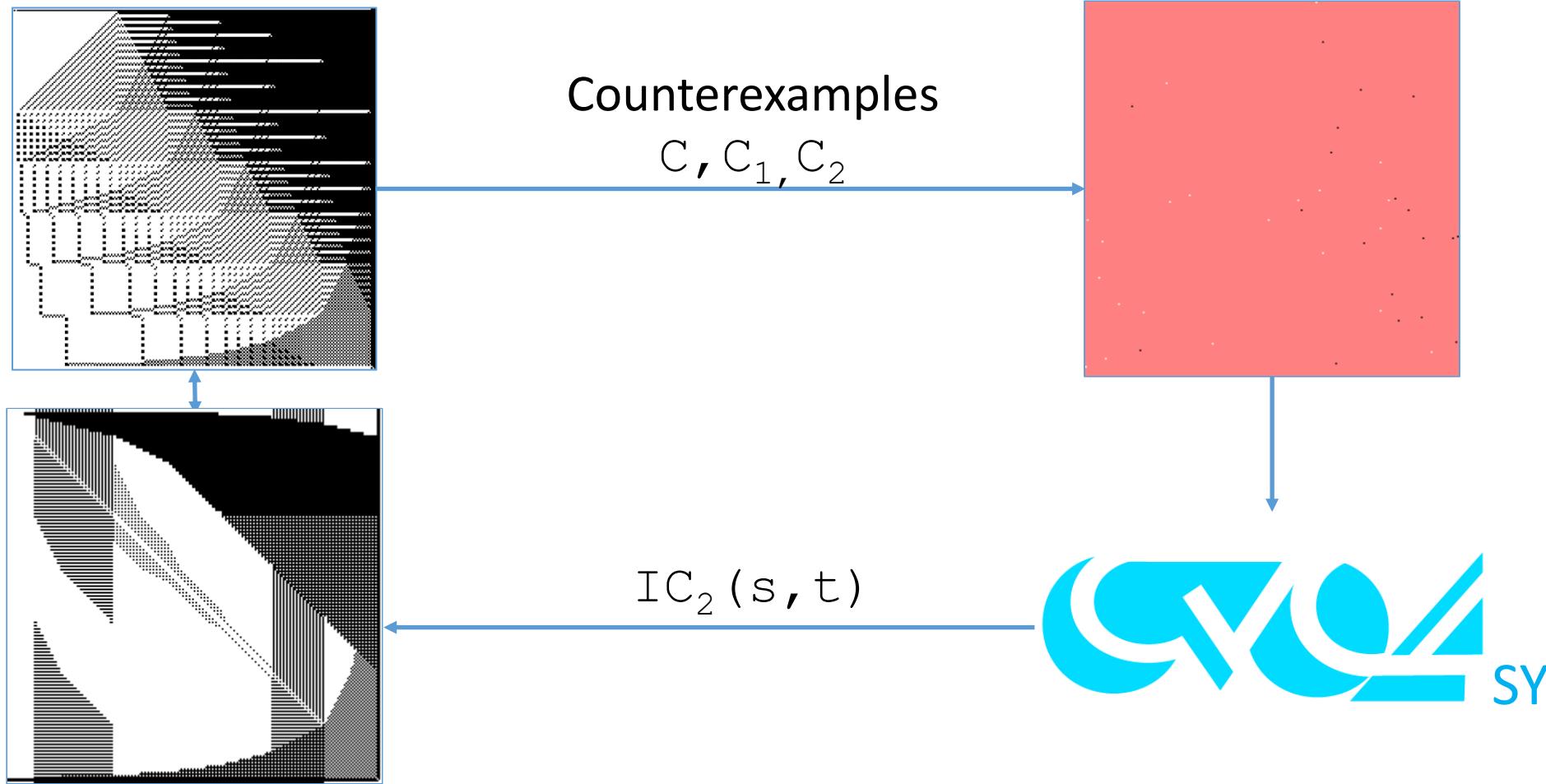


$IC_1(s, t)$

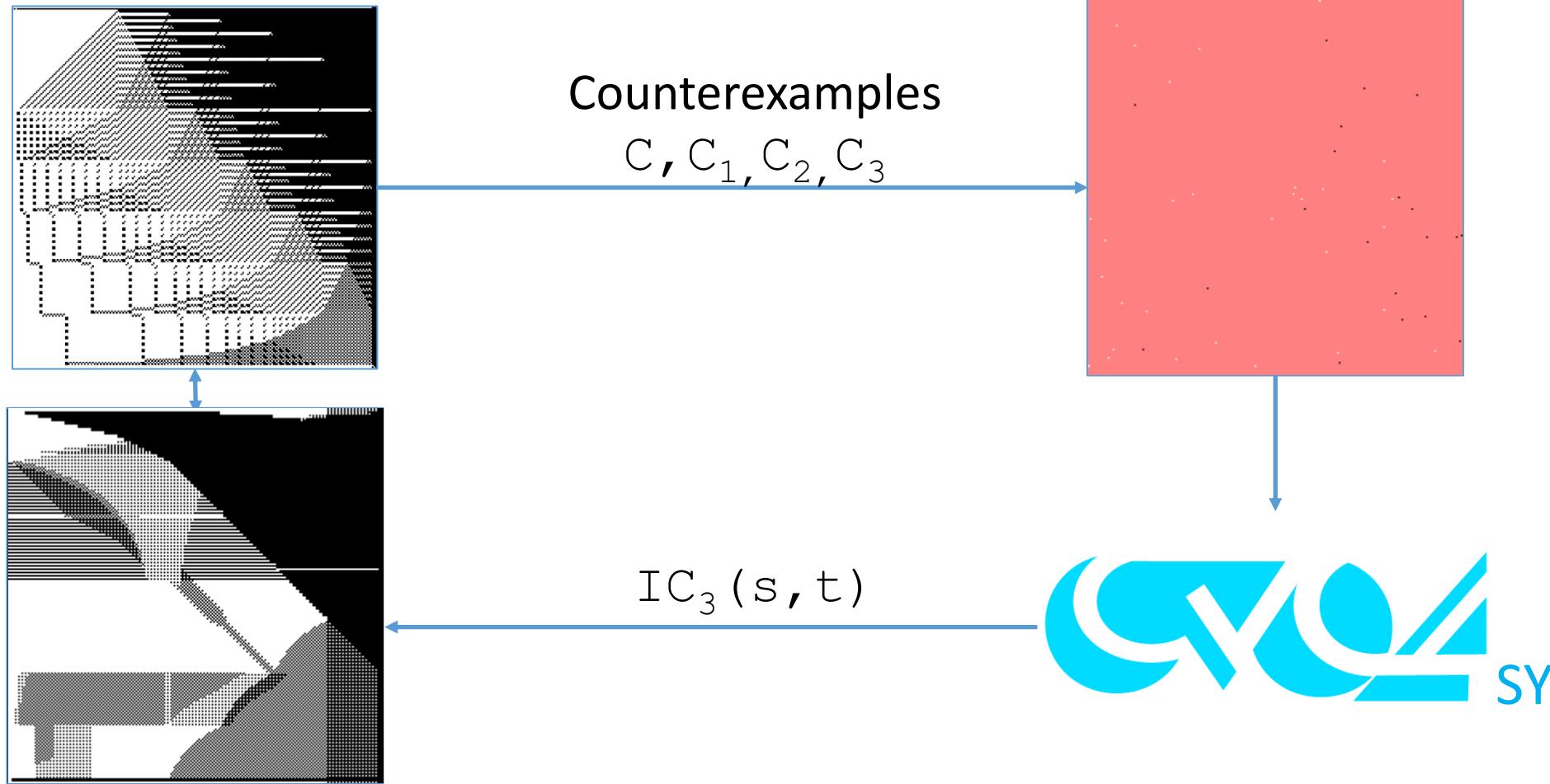
Synthesizing Invertibility Conditions



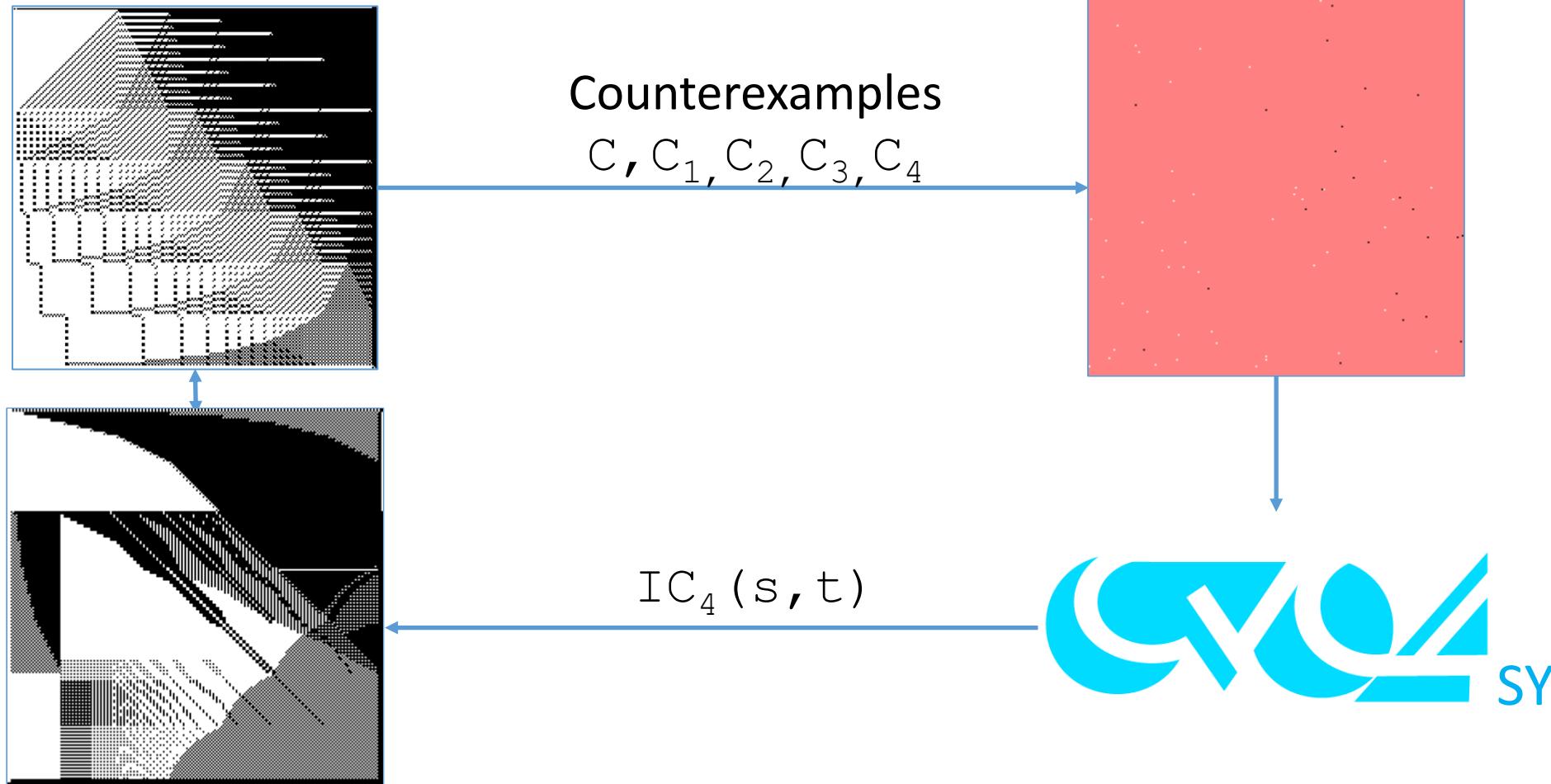
Synthesizing Invertibility Conditions



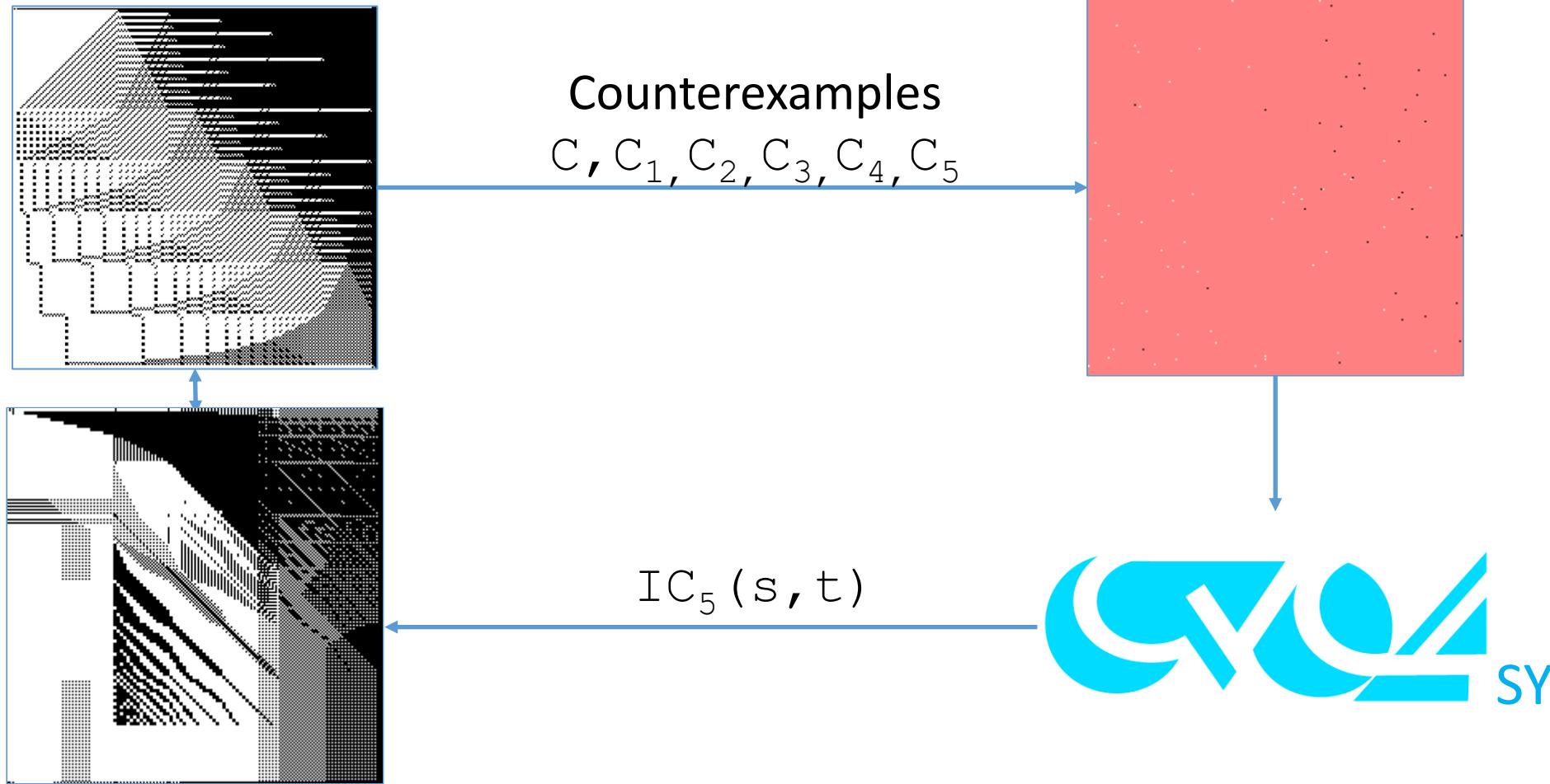
Synthesizing Invertibility Conditions



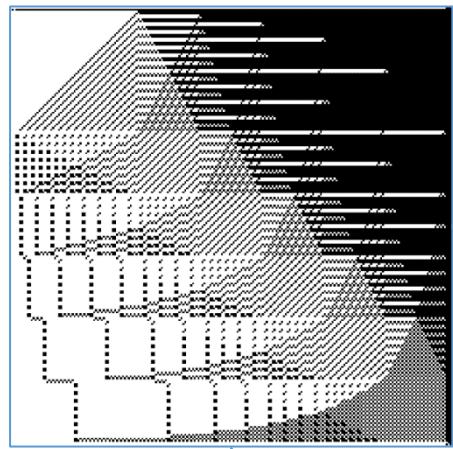
Synthesizing Invertibility Conditions



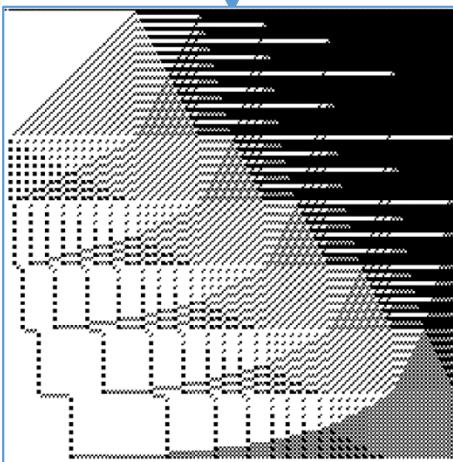
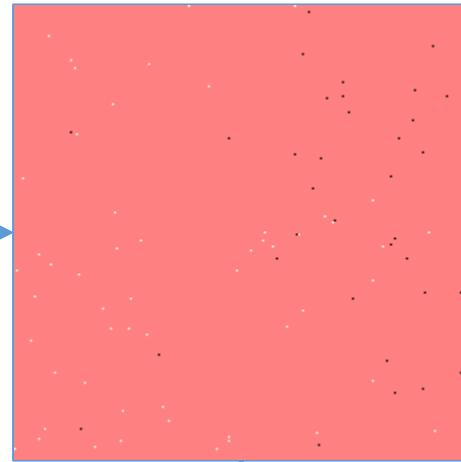
Synthesizing Invertibility Conditions



Synthesizing Invertibility Conditions



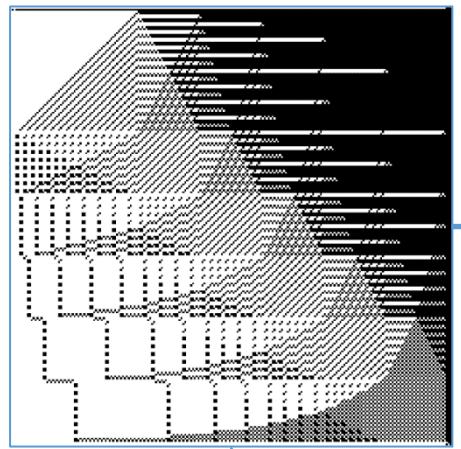
Counterexamples
 $C, C_1, C_2, C_3, C_4, C_5, C_6$



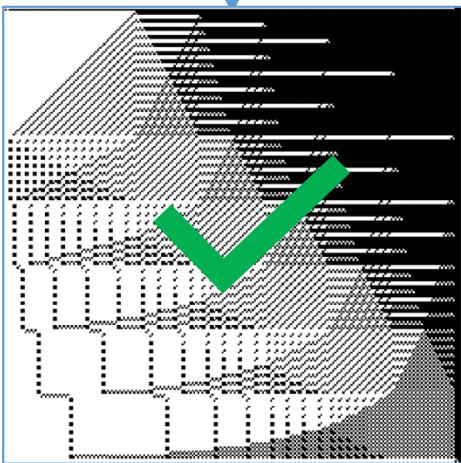
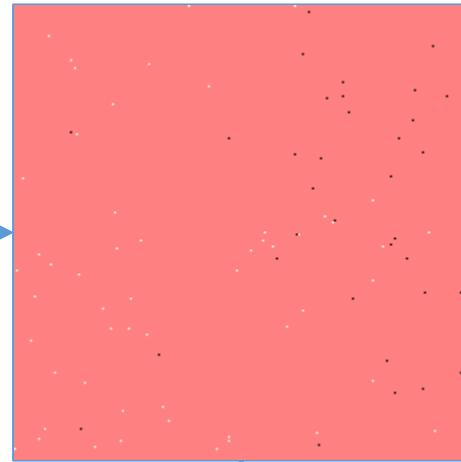
$$t \approx (t - s) \xrightarrow{\text{RTP}} + s \vee t \approx (t - s) \xrightarrow{\text{RTN}} + s \approx t$$



Synthesizing Invertibility Conditions



Counterexamples
 $C, C_1, C_2, C_3, C_4, C_5, C_6$



$$t \approx (t - s) \xrightarrow{\text{RTP}} s \vee t \approx (t - s) \xrightarrow{\text{RTN}} s \vee s \approx t$$



Finding Invertibility Conditions: Results

- In total, found **167 of 188** conditions

Finding Invertibility Conditions: Results

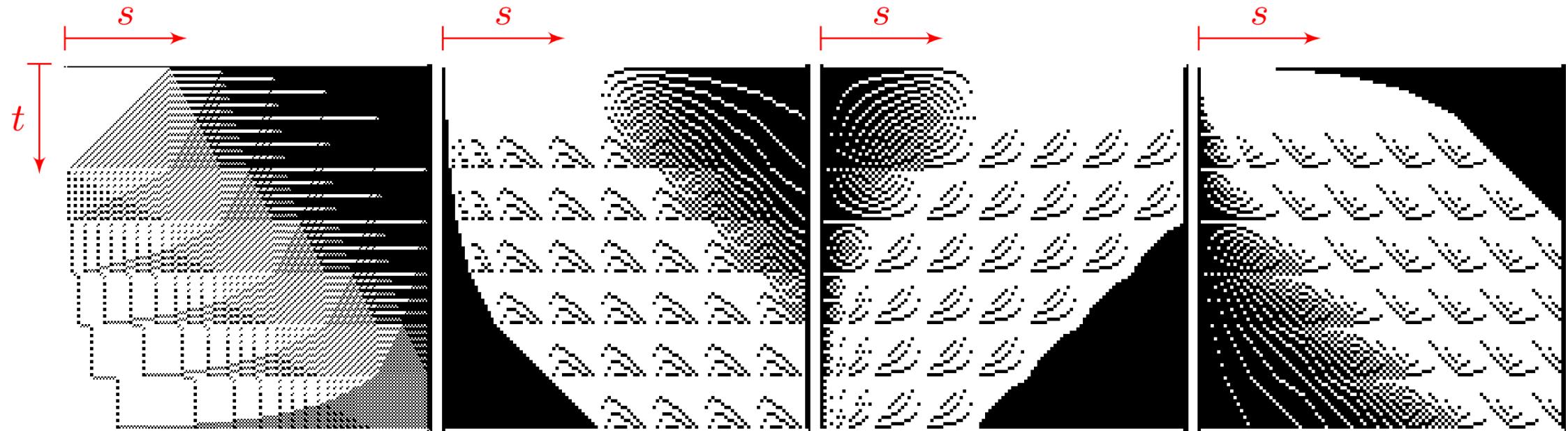
- In total, found **167 of 188** conditions

$$x \oplus s \sim t$$

- 14 choices for argument positions of \oplus
 - $\text{add}_1, \text{sub}_{1,2}, \text{mult}_1, \text{div}_{1,2}, \text{rem}_{1,2}, \text{fma}_{1,3}, \text{sqrt}_1, \text{abs}_1, \text{neg}_1, \text{roundToIntegral}_1$
 - 13 choices for \sim
 - $=, \neq, \geq, >, <, \leq, \text{isNormal}, \text{isSubnormal}, \text{isZero}, \text{isInfinite}, \text{isNaN}, \text{isPositive}, \text{isNegative}$
 - 7 additional ICs for equations with only a relation, e.g. $x > t$
- $\Rightarrow 14 * 13 + 7 = 188$
- When applicable, ICs hold for each 5 rounding modes {RNE, RNA, RTP, RTN, RTZ} of operator

Finding Invertibility Conditions: Results

- In total, found **167 of 188** conditions



(a) $x + s \approx t$

$$t \approx (t - s)^{\text{RTP}} + s \vee t \approx (t - s)^{\text{RTN}} + s \vee s \approx t$$
$$t \approx (t \div s)^{\text{RTP}} \cdot s \vee t \approx (t \div s)^{\text{RTN}} \cdot s \vee (s \approx \pm\infty \wedge t \approx \pm\infty) \vee (s \approx \pm 0 \wedge t \approx \pm 0)$$

(b) $x \cdot s \approx t$

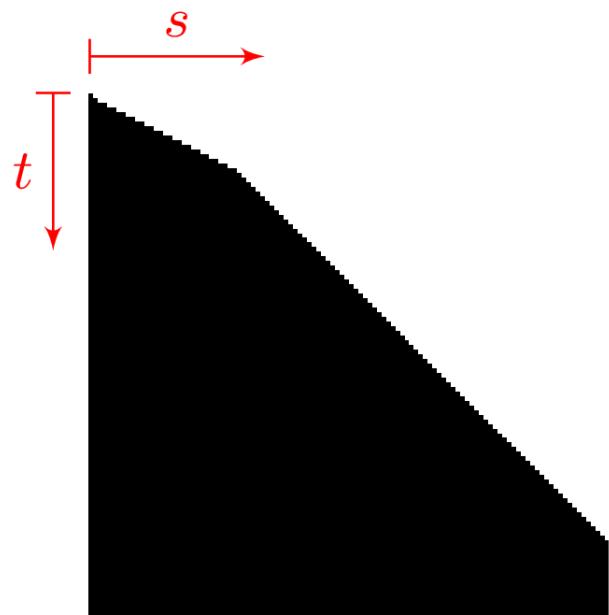
$$t \approx (s^{\text{RTP}} \cdot t)^{\text{RTP}} \div s \vee t \approx (s^{\text{RTN}} \cdot t)^{\text{RTN}} \div s \vee (s \approx \pm\infty \wedge t \approx \pm 0) \vee (t \approx \pm\infty \wedge s \approx \pm 0)$$
$$t \approx s^{\text{RTP}} \div (s \div t) \vee t \approx s^{\text{RTN}} \div (s \div t) \vee (s \approx \pm\infty \wedge t \approx \pm\infty) \vee (s \approx \pm 0 \wedge t \approx \pm 0)$$

(c) $s \div x \approx t$

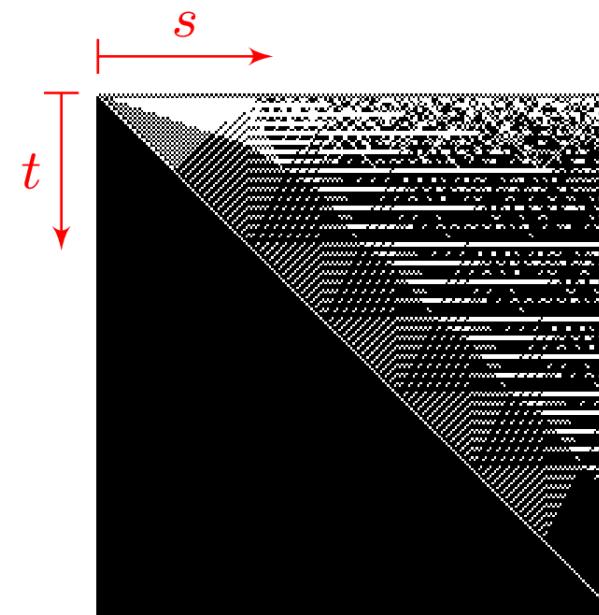
(d) $x \div s \approx t$

Finding Invertibility Conditions: Results

- Others were **hard to find**



(a) $x \text{ rem } s \approx t$



(b) $s \text{ rem } x \approx t$

$$\boxed{|t + t| \stackrel{\text{RTP}}{\leq} |s| \vee |t + t| \stackrel{\text{RTN}}{\leq} |s| \vee \text{ite}(t \approx \pm 0, s \not\approx \pm 0, t \not\approx \pm \infty)}$$

???

...behavior is pseudo-random!

Do Invertibility Conditions hold for all FP Formats?

- We **checked** all 167 invertibility conditions on other FP Formats
 - Targeted formats $\text{FP}_{3,5}$, $\text{FP}_{4,5}$, $\text{FP}_{4,6}$, $\text{FP}_{5,11}$, $\text{FP}_{8,24}$, $\text{FP}_{11,53}$
 - All invertibility conditions (appear to) generalize to all formats
 - **Successful in 94.5%** of the above cases using CVC4, Z3 (failures due to timeouts)
 - Approximately 32 days of compute time
- Future work: Format-Independent Verification!

What can we do with Invertibility Conditions?

- Summary of intuition:

$$\exists x. x \stackrel{R}{+} s \approx t$$

What can we do with Invertibility Conditions?

- Summary of intuition:

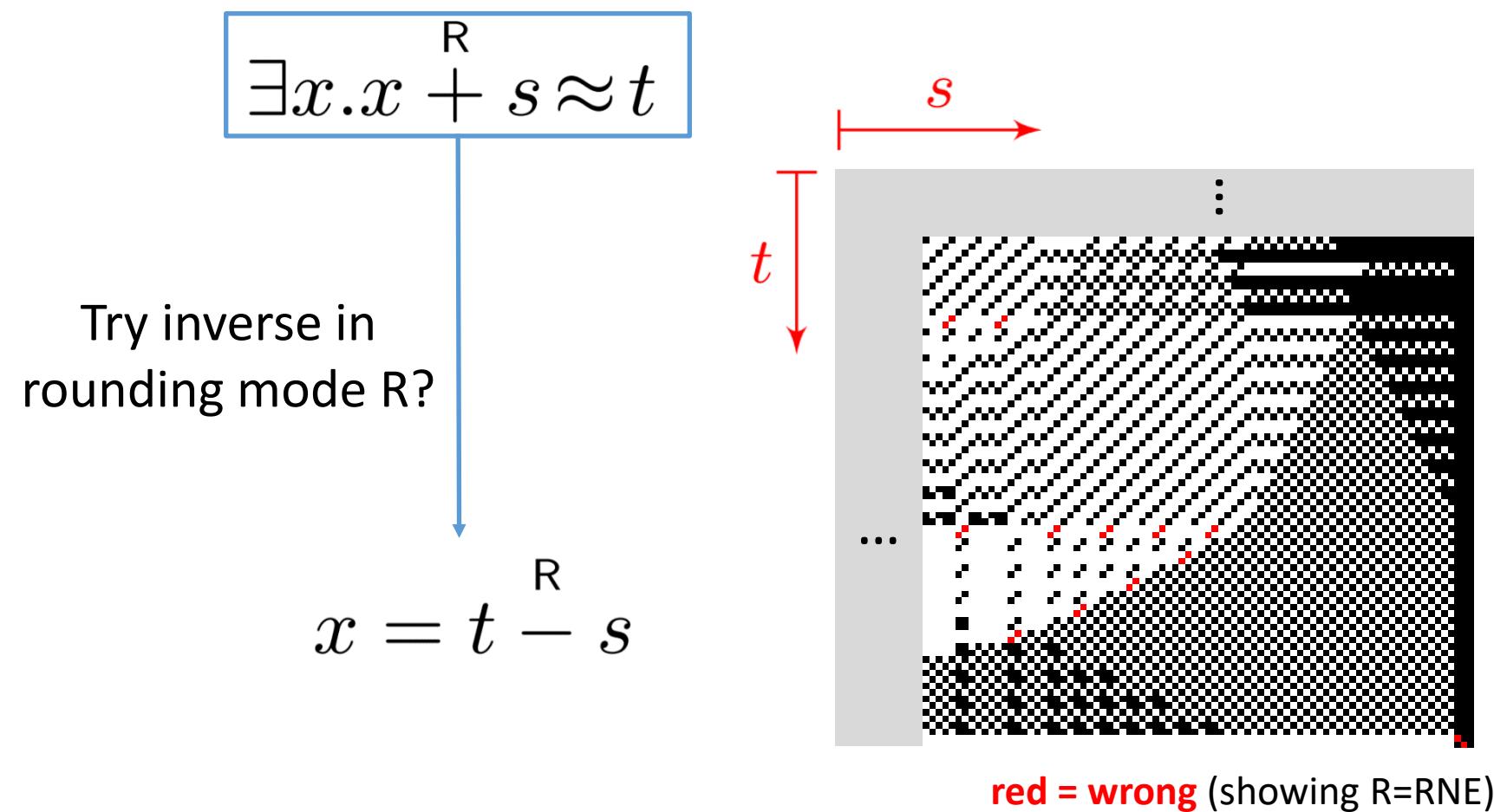
$$\boxed{\exists x. x + s \stackrel{R}{\approx} t}$$

Try inverse in
rounding mode R?

$$x = t - s$$

What can we do with Invertibility Conditions?

- Summary of intuition:



What can we do with Invertibility Conditions?

- Summary of intuition:

$$\exists x. x \stackrel{R}{+} s \approx t$$

What can we do with Invertibility Conditions?

- Summary of intuition:

$$\boxed{\exists x. \overset{R}{x + s \approx t}}$$
$$\Updownarrow$$
$$(t \overset{\text{RTP}}{-} s) \overset{R}{+ s \approx t} \vee (t - s \overset{\text{RTN}}{-} s) \overset{R}{+ s \approx t} \vee s \approx t$$

What can we do with Invertibility Conditions?

- Summary of intuition:

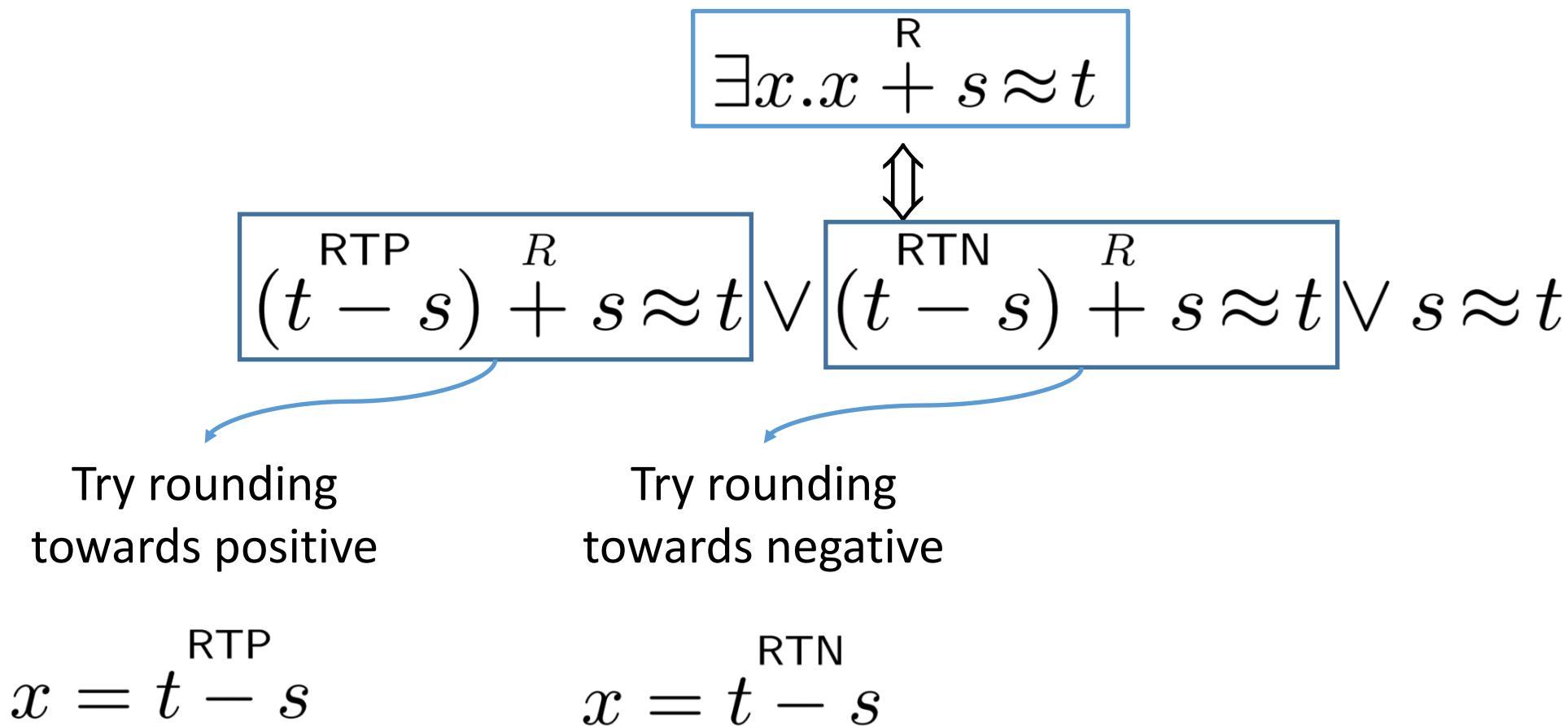
$$\begin{array}{c} \boxed{\exists x. x + s \stackrel{R}{\approx} t} \\ \Updownarrow \\ \boxed{(t - s) + s \stackrel{RTP}{\approx} t} \vee (t - s) + s \stackrel{RTN}{\approx} t \vee s \approx t \end{array}$$

Try rounding
towards positive

$$x = \stackrel{RTP}{t - s}$$

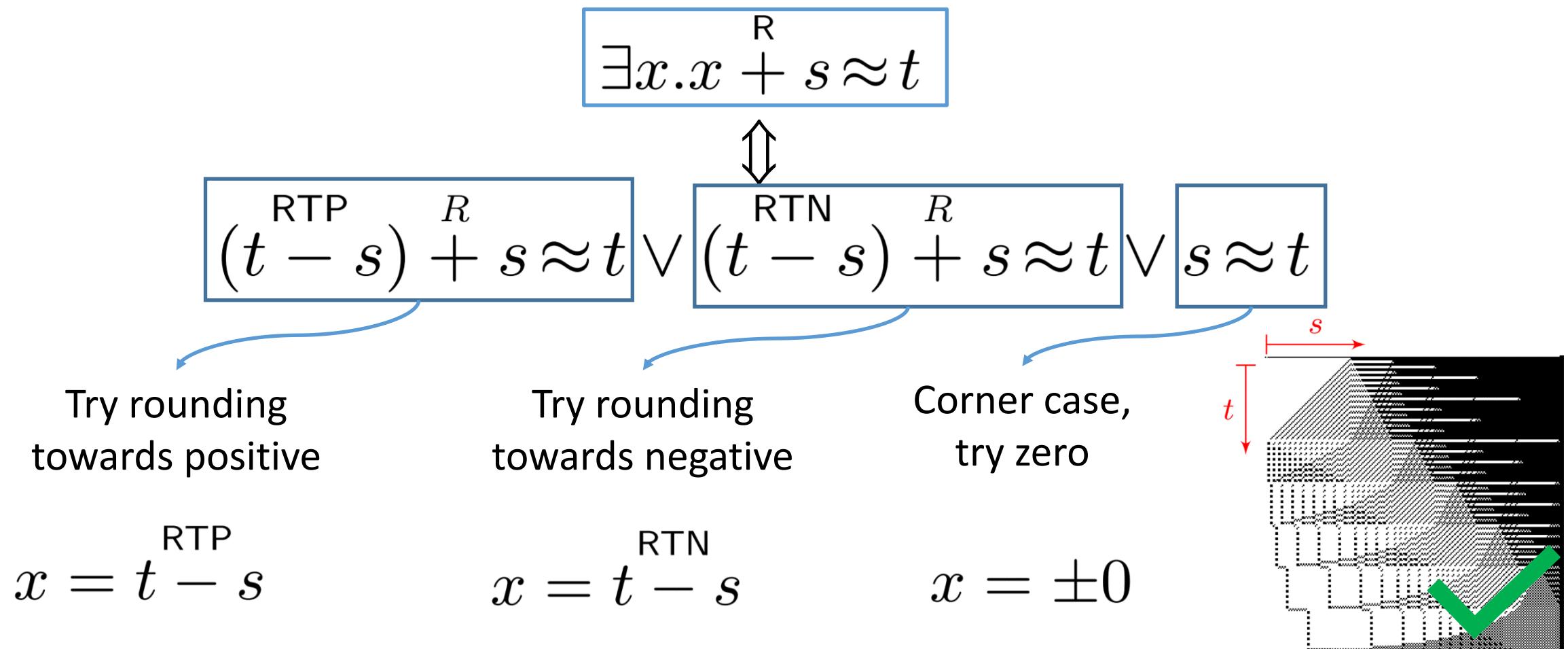
What can we do with Invertibility Conditions?

- Summary of intuition:



What can we do with Invertibility Conditions?

- Summary of intuition:



What can we do with Invertibility Conditions?

- Similar intuition for many other invertibility conditions:

Equation	Set of Possible Solutions	
$x \stackrel{R}{\cdot} s \approx t$	$x \in \{t \stackrel{\text{RTP}}{\div} s, t \stackrel{\text{RTN}}{\div} s\}$	
$x \stackrel{R}{\div} s \approx t$	$x \in \{t \stackrel{\text{RTP}}{\cdot} s, t \stackrel{\text{RTN}}{\cdot} s\}$	
$s \stackrel{R}{\div} x \approx t$	$x \in \{s \stackrel{\text{RTP}}{\div} t, s \stackrel{\text{RTN}}{\div} t\}$	+ corner cases for $\pm 0, \pm \infty, \text{NaN}$
$\sqrt[R]{x} \approx t$	$x \in \{t \stackrel{\text{RTP}}{\cdot} t, t \stackrel{\text{RTN}}{\cdot} t\}$	
$\text{fma}(x, s, t) \approx \pm 0$	$x \in \{-(t \stackrel{\text{RTP}}{\div} s), -(t \stackrel{\text{RTN}}{\div} s)\}$	

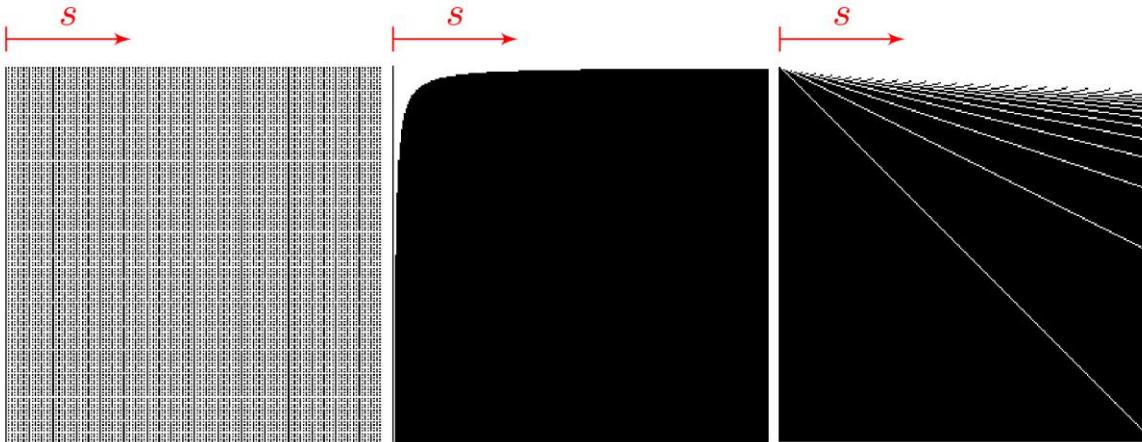
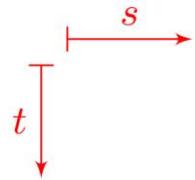
Ongoing Work

- Further rewrite rules, test case generation
- Solving algorithms based on invertibility conditions
 - Quantifier Elimination
 - Local search techniques [\[Niemetz et al CAV2016\]](#)
 - Quantifier Instantiation for Synthesis (for BV, FP, ...)
 - Quantifier instantiation procedures \Leftrightarrow synthesis procedures
- Bit-width independent verification of invertibility conditions
 - Initial work “Toward Bit-Width Independent Proofs in SMT Solvers” [\[CADE 2019\]](#)
- Other applications: Syntax-guided optimization of FP code?
- ...Your application here

Thanks for Listening!

- Techniques in talk available in SMT solver cvc5
 - Open-source : <https://cvc5.github.io/>
- Questions?

Visualizing Invertibility Conditions for Bit-Vectors

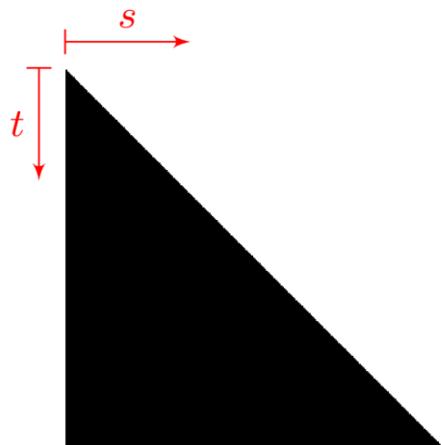


(a) $x + s \approx t$

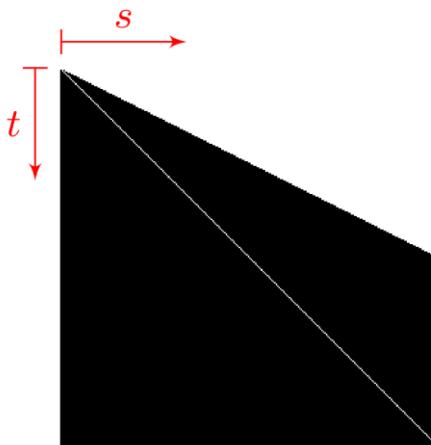
(b) $x \cdot s \approx t$

(c) $s \div x \approx t$

(d) $x \div s \approx t$



(a) $x \text{ rem } s \approx t$



(b) $s \text{ rem } x \approx t$

White = IC is true
Black = IC is false
(shown for 8-bit)