

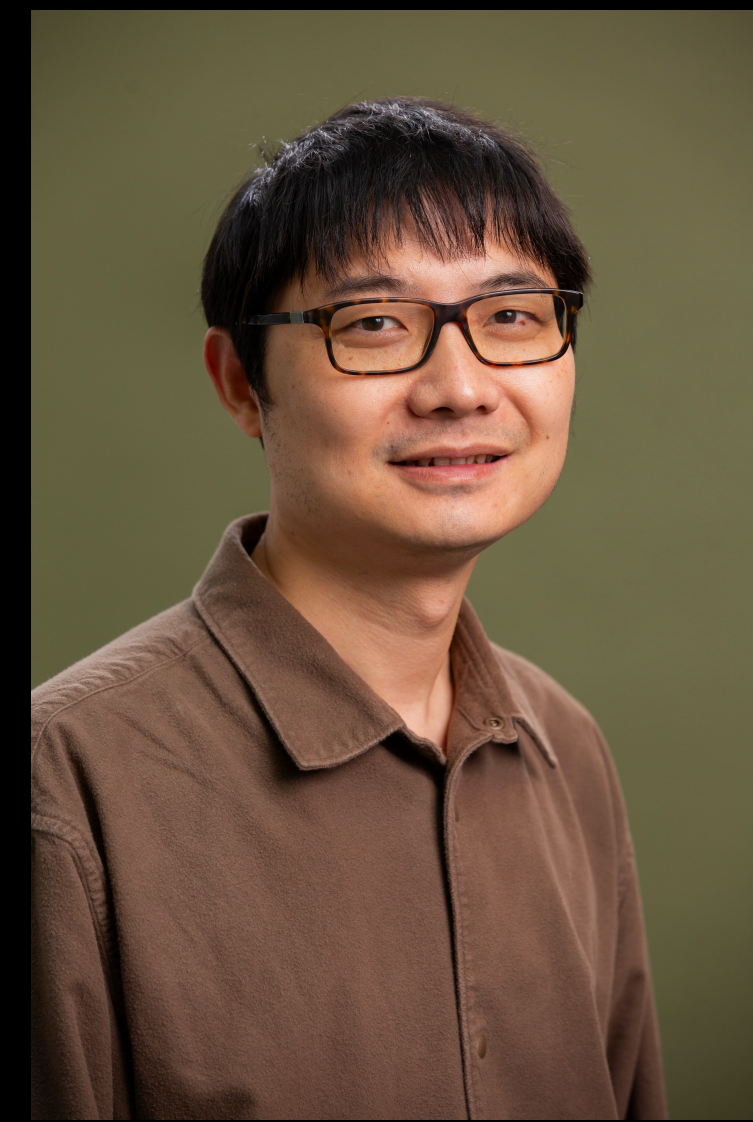
# FMitF: Track I: Flexible Data Plane Programming

Award ID # 2319425

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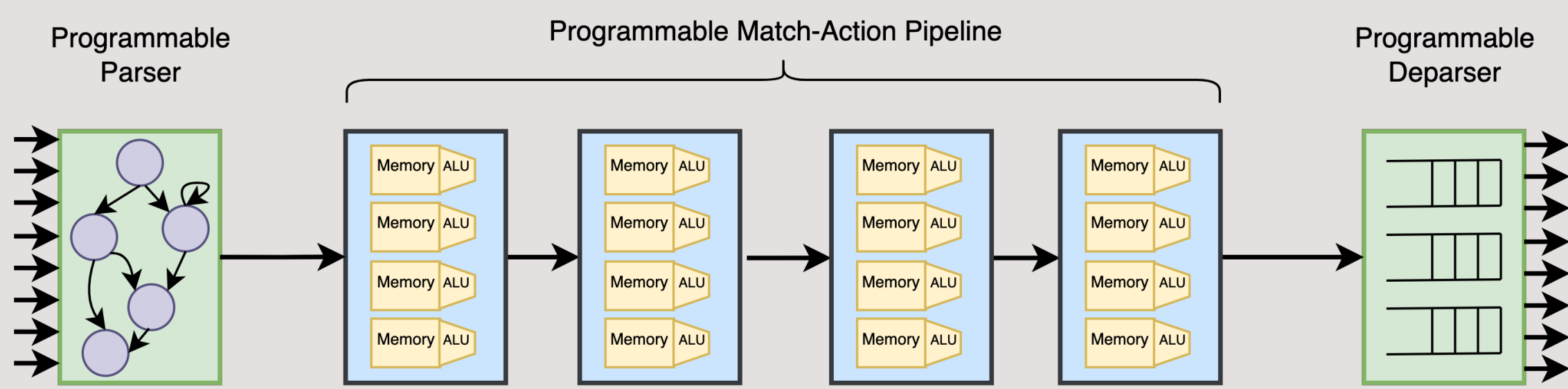
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URL: [https://purdue-isl.github.io/projects\\_pages/Program-Synthesis-Approach](https://purdue-isl.github.io/projects_pages/Program-Synthesis-Approach)



## Motivation

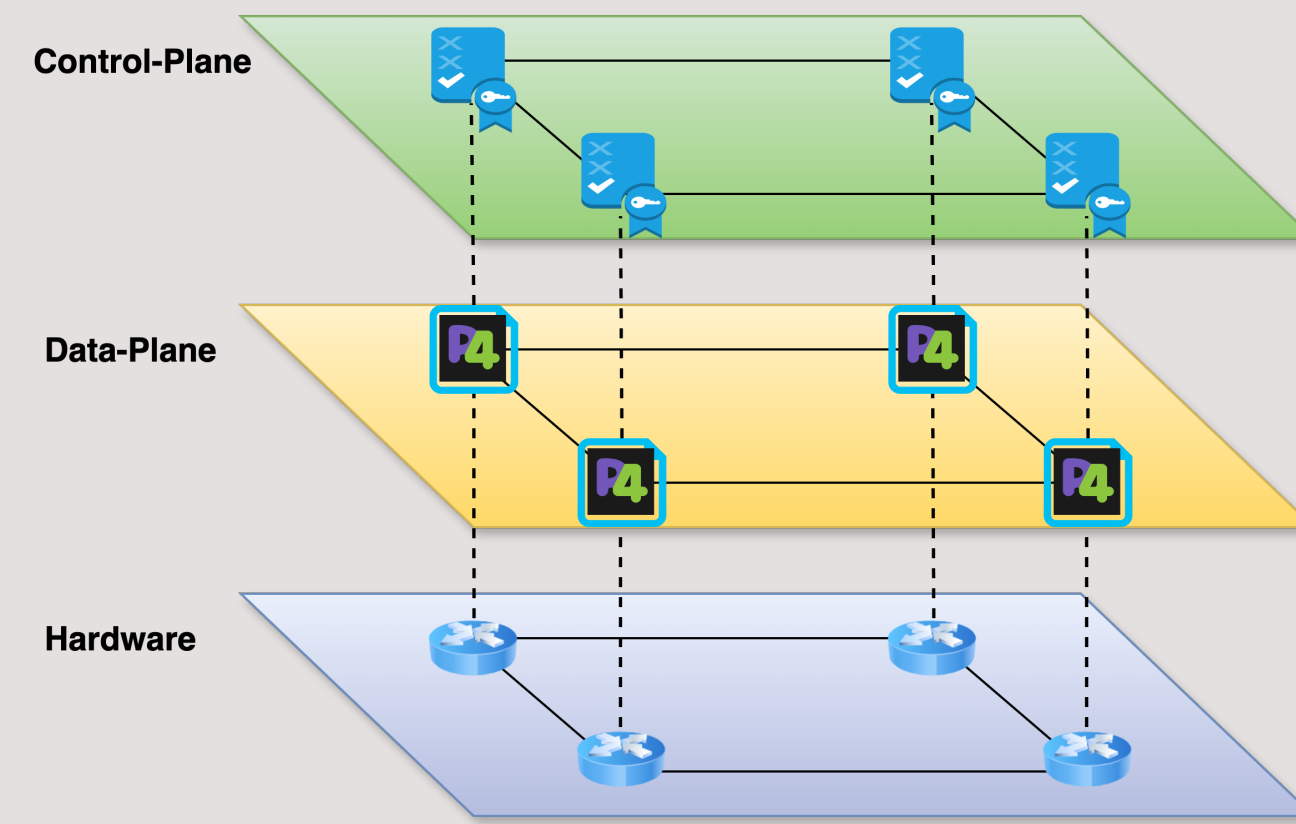
### Programmable Switches Architecture



Hard to program with low-level, hardware-specific constraints

- Limited number of stages
- Limited memory - SRAM and TCAM, etc.

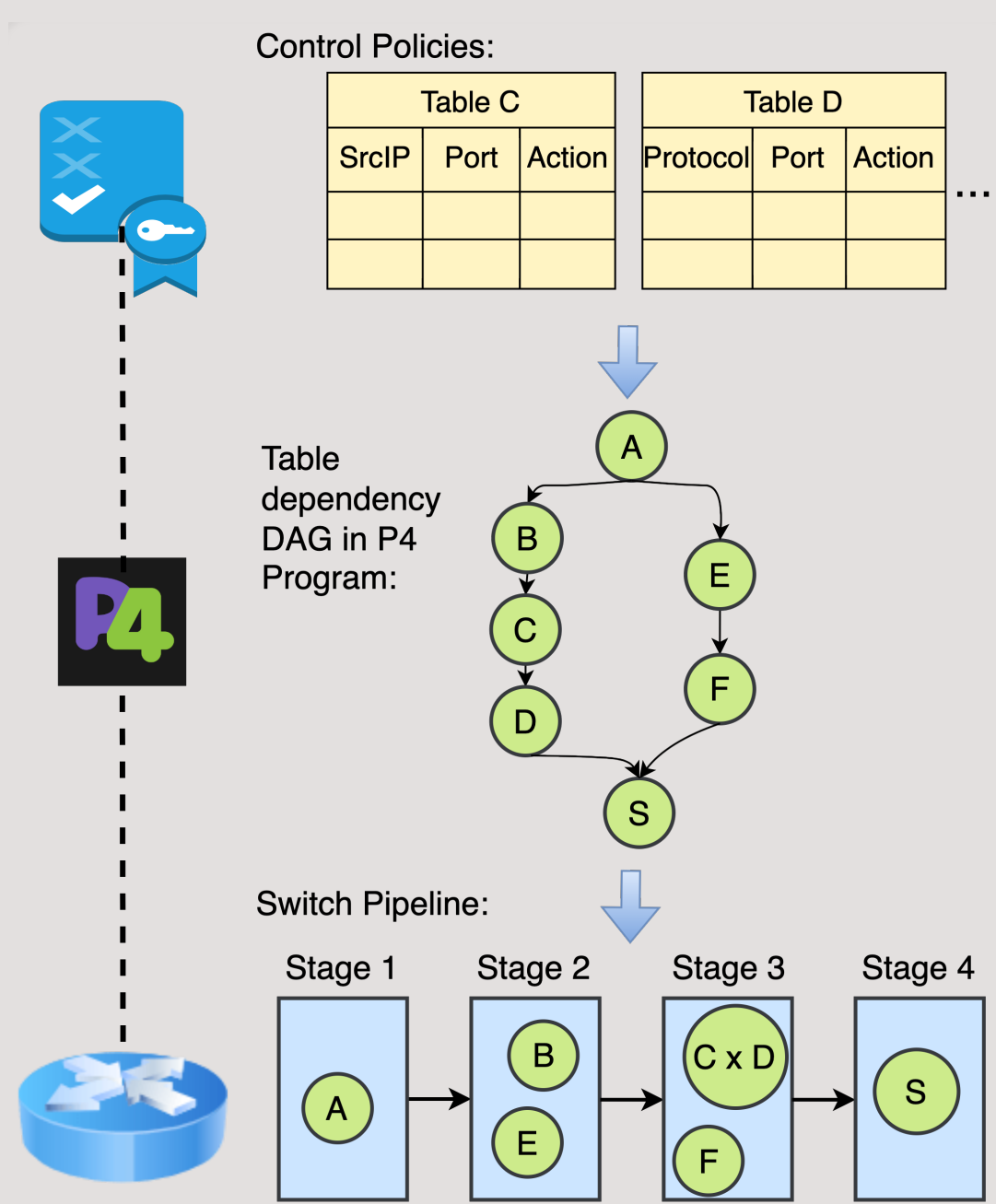
### P4 programming



Lack of support for customizable optimization

- Flexible optimization targets (latency, resource allocation, etc.)
- Network-wide optimization
- Accommodation to specific control plane and hardware

## Challenges



### How to make data plane programming more flexible?

- Describing control plane and hardware assumptions
- Describing global optimization targets

### How can formal methods help achieve efficient compile-time optimizations?

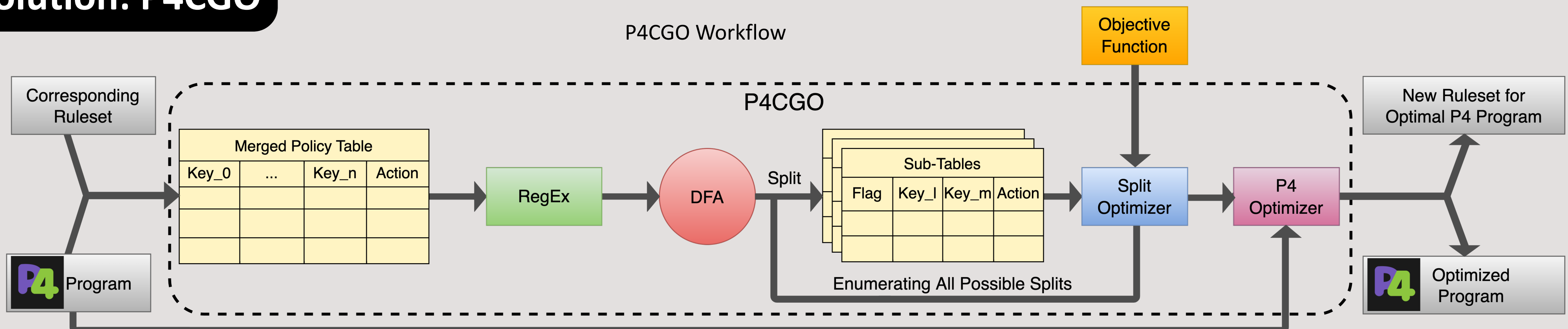
- Leveraging domain knowledge
- Enhancing generic synthesis techniques

## Scientific Impact

- The project will advance formal methods and program synthesis, contributing to areas such as *syntax-guided synthesis*, *quantitative synthesis*, and *specification mining*
- Our tools will simplify data plane programming, making formal reasoning and optimization easier and tractable
- Our methods could have broader applications (e.g., many other optimization problems) and benefit users beyond the networking domain
- Preliminary results published: Wen, C., Li, Z., Jafri, S.U., Qiu, X. and Rao, S. 2024. P4CGO: Control Plane Guided P4 Program Optimization. In *2024 SIGCOMM Workshop on Formal Methods Aided Network Operation (FMANO '24)*, pp. 1-7.

## Our Solution: P4CGO

### P4CGO Workflow

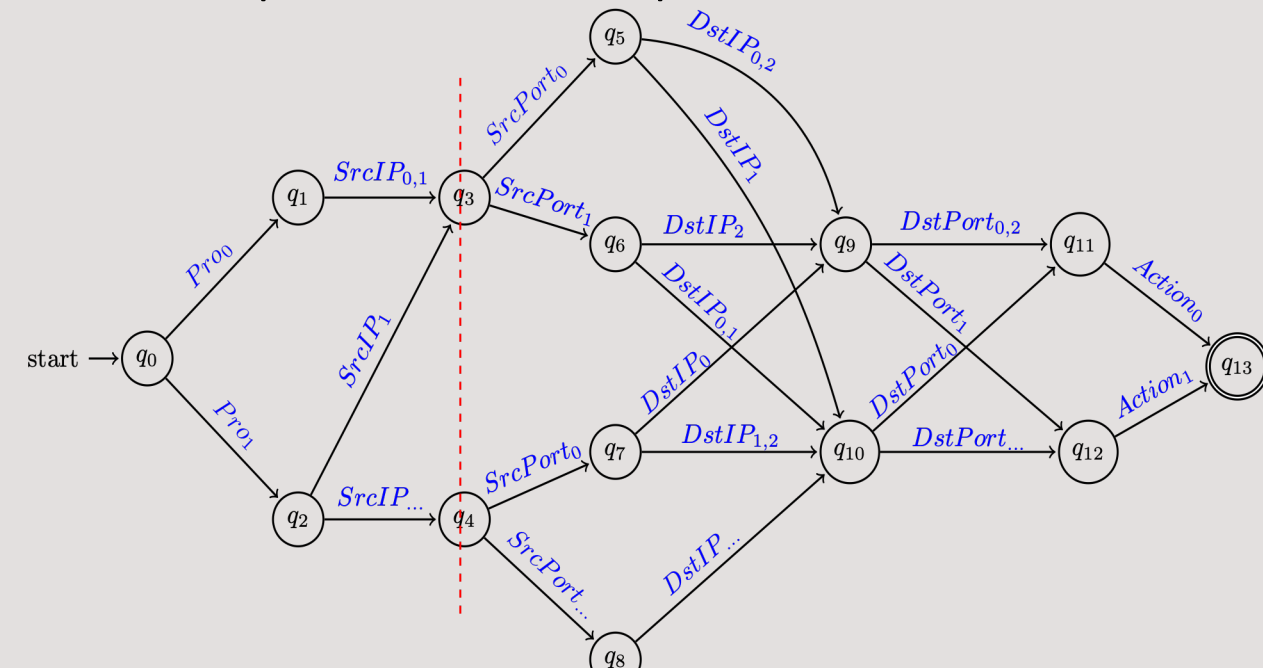


Take P4 program together with control plane policy and objective function as input

merged-policy-table (size 165)				
Src_IP	Src_Port	Dst_IP	Dst_Port	Action
192.14.4.1/32	445	172.31.255.2/32	161	drop
131.5.0.0/16	134	*	161	permit
...	...	...	...	...
*	*	*	*	drop

minimize (SRAM + TCAM)

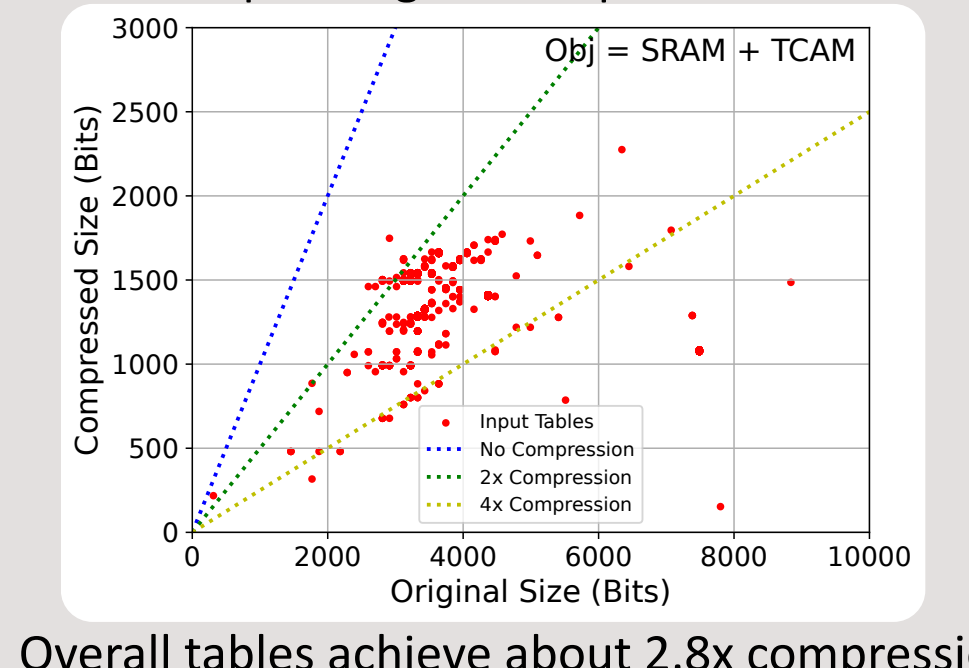
Transform inputs into a DFA to perform minimization and DFA split



Generate optimized P4 program with corresponding control plane

sub-table-1 (size 25)			
Flag	Dst_IP	Dst_Port	Action
F1	172.31.255.2	161	drop
F0	*	161	permit
...	...	...	...
*	*	*	drop

sub-table-2 (size 16)			
Src_IP	Src_Port	Action	Flag
192.14.4.1/32	445	Flag = F1	*
131.5.0.0/16	134	Flag = F0	*
...	...	...	...
*	*	Flag = F1	*



## Impact on Society

Simplifying data plane programming will promote the broader adoption of programmable routers, benefiting the networking and IT industries.

## Impact on Education

Curriculum development will include new material on programmable switches and networking for courses at Purdue.

## Broader Participation

- This project has been providing valuable training for four graduate students and one undergraduate student
- We have been extensively interacting with Purdue's IT department

